Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**M. E. Sem – IV Examination May 2011**

**Subject code: 740301**

**Subject Name: Advance VLSI Design**

**Date:16/05/2011** **Time: 10.30 am – 01.00 pm**

**Total Marks: 70**

## Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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|---|---|---|---|
| **Q.1** | **(a)** | Explain Flatten Logic Structures for timing in Architecting Speed. | **07** |
| | **(b)** | Discuss impact of reset on area in general, and Resources without reset in particular. | **07** |
| **Q.2** | **(a)** | Explain the issues related to gated clock in Architecting Power. | **07** |
| | **(b)** | Briefly explain software/hardware co-design. | **07** |
| | | **OR** | |
| | **(b)** | Define Metastability and describe Metastability caused by timing violation. | **07** |
| **Q.3** | **(a)** | Discuss resource sharing in FPGA | **07** |
| | **(b)** | List various power management techniques and discuss input control in detail. | **07** |
| | | **OR** | |
| **Q.3** | **(a)** | Briefly explain Graphical State machines. | **07** |
| | **(b)** | Expalin any two solution of metastability problem. | **07** |
| **Q.4** | **(a)** | Discuss Asynchronous Assertion, Synchronous Deassertion for reset circuit. | **07** |
| | **(b)** | In decision tree, draw and discuss following:<br>(1) Simple priority with serialized Mux structure (2) Priority-encoded logic | **07** |
| | | **OR** | |
| **Q.4** | **(a)** | Explain potential hazard on reset pin, and draw waveform with reset hazard in internally generated reset. | **07** |
| | **(b)** | Discuss Combinatorial Loops in detail. | **07** |
| **Q.5** | **(a)** | Explain Partitioning in general; and Data Path Versus Controlling in particular. | **07** |
| | **(b)** | Define or briefly discuss following:<br>1. Floor planning<br>2. Rise and fall time of signal<br>3. ASIC<br>4. Fully asynchronous reset<br>5. Latency<br>6. Throughput<br>7. Dynamic power consumption in CMOS | **07** |
| | | **OR** | |
| **Q.5** | **(a)** | Discuss speed versus area in synthesis optimization. | **07** |
| | **(b)** | Explain the effect of reset on register balancing | **07** |

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