

**GUJARAT TECHNOLOGICAL UNIVERSITY**

M.E Sem-I Remedial Examination January/ February 2011

**Subject code: 710403****Subject Name: ASIC Design****Date: 02 /02 /2011****Time: 02.30 pm – 05.00 pm****Total Marks: 60****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1 (a)** Describe logical design and physical design steps in ASIC design flow with block diagram. **06**
- (b)** Write the VHDL code for the 4 to 16 decoder using behavioral style of modeling. **06**
- Q.2 (a)** Do as directed: **06**
- (1) Whether following statement is true or false. “Nested process statements are possible in VHDL”. Also justify your answer.
  - (2) List all different subtypes of scalar data types in VHDL.
  - (3) Discuss necessity of resolution function.
- (b)** Draw the basic block diagram of any CPLD and discuss. **06**
- OR**
- (b)** Explain in brief (1) Channeled Gate array (2) Channel less gate array (3) Structured gate array **06**
- Q.3 (a)** Explain Inertial Delay model with suitable example. Also summaries effect of Inertial Delay on Signal Drivers. **06**
- (b)** (1) Compare Signal and Variable in VHDL (2) Discuss Block statement in VHDL **06**
- OR**
- Q.3 (a)** Define the following terms: **06**
1. Configuration declaration in VHDL
  2. Transport Delay Model
  3. Sequential Signal assignment statements
  4. Component Instantiation
  5. Data flow modeling
  6. Anti-fuse technology
- (b)** Write the VHDL code using structural model for a 9-bit parity generator circuit. **06**
- Q.4 (a)** List the main purposes of test-bench. Discuss waveform generation using test-bench. **06**
- (b)** Discuss modeling of mealy state machine with suitable example. **06**
- OR**
- Q.4 (a)** Do as directed: **06**
- (1) Differentiate between exit and next statements.
  - (2) Briefly describe necessity of Configuration.
  - (3) Elaborate Package declaration
- (b)** Compare following: **06**
- (1) PLA and ROM
  - (2) FPGA and CPLD
- Q.5 (a)** Explain following operators used in VHDL with example **06**
- (1) rem (2) mod (3) abs
- (b)** Briefly describe implicit and explicit visibility in VHDL. **06**
- OR**
- Q.5 (a)** How many functions of how many variables can be realized by a PLA with n inputs and m outputs? **06**
- Realize the following functions using PLA.
- $$F1 = \sum m(0,1,4,6)$$
- $$F2 = \sum m(2,3,4,6,7)$$
- $$F3 = \sum m(0,1,2,6)$$
- $$F4 = \sum m(2,3,5,6,7)$$
- (b)** Write a short note on Floor planning and Placement. **06**

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