Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME Semester –II Examination Dec. - 2011

Subject code: 1710412 **Date: 23/12/2011**

Subject Name: Digital VLSI Design

Time: 02.30 pm – 05.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions. 2. Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Define threshold voltage for MOS transistor. Describe the four component of threshold voltage.	**07**
	(b)	Explain the importance of Regular, Modular and Local Architecture for VLSI. Also give one example for each.	**07**
Q.2	**(a)**	Explain the need for LOCOS Process, principle of LOCOS and LOCOS process with necessary diagram.	**07**
	(b)	Derive the Drain current equation for $V_{DS} > V_{Dsat}$.	**07**
		OR	
	(b)	Explain Oxidation and Photolithography process for MOS fabrication.	**07**
Q.3	**(a)**	Describe Accumulation, Depletion and Inversion process for the MOS system under external bias. Also derive the equation for maximum depletion region depth at the onset of surface inversion.	**07**
	(b)	Write short note on MOSFET scaling.	**07**
		OR	
Q.3	**(a)**	Explain flat-band voltage in terms of MOS structure with necessary energy band diagrams.	**07**
	(b)	Write short note on Layout Design Rules.	**07**
Q.4	**(a)**	What is CPL. Draw the circuit diagram of CPL NAND2 and CPL NOR2 gate and explain working.	**07**
	(b)	Consider a resistive-load inverter circuit with V_{DD}= 5V, k_n'= 22 μA/V^2, V_{T0} = 0.7 V, R_L = = 200 kΩ, and W/L = 2. Calculate the critical voltages $(V_{OL}, V_{OH}, V_{IL}, V_{IH})$ on the VTC and find the noise margins of the circuit.	**07**
		OR	
Q.4	**(a)**	Derive switching threshold voltage for CMOS 2-input NOR gate circuit. Compare it with CMOS inverter threshold voltage. Comment on them.	**07**
	(b)	Compute the ratio between nMOS and pMOS transistor width to obtain a symmetric inverter for 0.18μ technology in which μ_n = 360 cm^2/V·s, μ_p = 109 cm^2/V·s, V_{Tn}=0.35 V and V_{Tp} = -0.36 V, with V_{DD} = 1.8 V.	**07**
Q.5	**(a)**	Define τ_{PHL} and τ_{PLH} for CMOS inverter. Derive τ_{PHL} for CMOS inverter.	**07**
	(b)	Explain the Euler path approach to find the optimized stick-diagram for any CMOS logic circuit. Take suitable example to justify the your answer.	**07**
		OR	
Q.5	**(a)**	Explain the charge sharing problem in DOMINO CMOS logic. How it can be over come, suggest simple solution.	**07**
	(b)	Write a short note on Pre-charge and Evaluate logic for dynamic logic circuits.	**07**

****