Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

ME Semester –II Examination Dec. - 2011

Subject code: 1722602 **Date: 12/12/2011**
Subject Name: CMOS Circuit Design II
Time: 02.30 pm – 05.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	With necessary figures explain Micropower Op-amps.	**07**
	(b)	Discuses the Speed and Noise Issues for References.	**07**
Q.2	**(a)**	Draw and explain the Generation of PTAT current using a simple amplifier.	**07**
	(b)	Sketch the schematic of an adaptive voltage follower that can source or sink current.	**07**
		OR	
	(b)	With necessary figures explain High-Speed Op-amps.	**07**
Q.3	**(a)**	Write a short note on Row/Colum Decoder.	**07**
	(b)	Explain the operation of Sense Amplifier with necessary figures.	**07**
		OR	
Q.3	**(a)**	Explain the operation of Decision Circuit.	**07**
	(b)	What is Jitter? Explain for PLL.	**07**
Q.4	**(a)**	Explain the problem of Lock Acquisition for PLL.	**07**
	(b)	Explain the operation of Parallel DAC.	**07**
		OR	
Q.4	**(a)**	Explain the operation of Serial ADC.	**07**
	(b)	Write a short note on Floating Gate Memory.	**07**
Q.5	**(a)**	Explain the effect of junction capacitance nonlinearity in Switched Capacitor Integrator.	**07**
	(b)	List different types of Switched-Capacitor Amplifier and Explain any one in detail.	**07**
		OR	
Q.5	**(a)**	Explain the operation of Monostable Multi Vibrator.	**07**
	(b)	Write a short note on Voltage Generators.	**07**

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