GUJARAT TECHNOLOGICAL UNIVERSITY
ME Semester –I Examination Feb. - 2012

Subject code: 710305N   **Date: 15/02/2012**
Subject Name: Programmable Logic Controller
Time: 10.30 am – 01.00 pm   **Total Marks: 70**

Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Design basic two-axis robot using following guidelines:- 1) Assume suitable configuration. 2) Draw schematic diagram. 3) Write event sequence. 4) Prepare operational matrix. 5) Draw PLC ladder logic diagram and show register patterns.	**09**
	(b)	Implement any one digital combinational circuit having 11 inputs and 1 output using PLC ladder logic diagram.	**05**
Q.2	**(a)**	Compare PLC with physical relay based control system. Draw and explain PLC system architecture with discrete input and discrete output modules.	**07**
	(b)	What is the difference between discrete I/O and digital I/O? Explain with the help of suitable examples.	**07**
		OR	
	(b)	Explain how PLC scans all inputs, executes the ladder logic diagram and updates the outputs, with the help of suitable industrial process example.	**07**
Q.3	**(a)**	Enumerate various types of PLC I/O modules. Justify the necessity of I/O modules and explain discrete AC input module.	**07**
	(b)	Is PLC same as or different from the data processing computers? Justify your answer.	**07**
		OR	
Q.3	**(a)**	Draw and explain PLC memory map for 2K x 2-byte RAM. Show address ranges in hexadecimal.	**07**
	(b)	Explain CPU processor with the help of functional block diagram.	**07**
Q.4	**(a)**	Explain construction and working of LVDT, which is one of the analog input devices to the PLC.	**07**
	(b)	Explain latch/unlatch function of PLC with suitable example. Whether it makes the PLC fail-safe or not? Justify your answer.	**07**
		OR	
Q.4	**(a)**	Explain PLC arithmetic functions.	**07**
	(b)	Explain PLC advanced comparison functions.	**07**

Q.5 (a) Explain PLC data handling functions which are used to move the data form single or multiple source locations to single or multiple destination locations, i.e. all types of possible data movement. **07**

(b) Prepare ladder logic diagrams for following processes: **07**

(1) A solenoid S, is to go on when count C goes up to 22, and when count D goes down from 37 to 0, and when count E goes up to 8. Furthermore, if count F goes down from 17 to 0 at any time, the solenoid is to be kept from operating. One stop button resets the entire process, including the solenoid being off.

(2) An output pulse, V, is to go ON 3.5 seconds after an input, W, is turned on. The V time-on interval is to last 7.5 seconds only. V is to go on again 3 seconds later for 5.3 seconds.

OR

Q.5 (a) Draw schematic diagram, list the process hardware, Prepare event sequence, construct Ladder Logic Diagram and show I/O connection details for the following process: **10**

In this process, the mixture of two liquids (in the tank) is to be filled in the bottles (underneath the tank), moving on the conveyor belt. Initially tank should be empty. Then 50% of the tank is to be filled with first liquid and remaining tank is to be filled with second liquid. Then mixture is to be stirred properly for 2 minutes. Then conveyor motor should be on until empty bottle comes exactly under the outlet valve of the tank. At that time the conveyor should stop and the outlet valve is to be open and kept open until the bottle is filled completely. Then the output valve is to be closed and conveyor should be on again till another empty bottle come underneath the outlet valve. This process of filling the empty bottles should be repeated until the tank becomes empty. At that time the whole process is to be repeated from the beginning. Assume suitable data and clearly mention them.

(b) Explain PLC analog signal processing. **04**

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