Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

ME Semester –I Examination Feb. - 2012

Subject code: 710412N **Date: 18/02/2012**

Subject Name: Digital VLSI Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Explain VLSI design flow with necessary diagrams and explain the concepts of regularity, modularity and locality with suitable example. **07**

(b) Discuss fabrication process of NMOS transistor in detail with required diagram. **07**

Q.2 **(a)** Draw energy band diagram of the combined MOS system. Explain MOS system under different external bias voltage with energy band diagram. **07**

(b) Derive the MOSFET drain current equation while MOSFET is operating in linear region. Draw the current-voltage characteristics of the MOSFET and explain in detail. **07**

OR

(b) Calculate the threshold voltage V_{T0} at $V_{SB} = 0$, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness t_{ox} = 500 Å, and oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2}. **07**

At room temperature, i.e., T = 300 K, take $n_i = 1.45 \times 10^{10}$ cm^{-3}, Boltzmann constant = 1.38×10^{-23} J/K, Electron charge = 1.6×10^{-19} C, Relative permittivity of Si = 11.68, Relative permittivity of Silicon dioxide = 3.97, and $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm. Assume ϕ_F (gate) = 0.55V

Q.3 **(a)** Draw the resistive-load nMOS inverter circuit and the voltage transfer characteristics with important points. Find the equation of all the critical voltages for the circuit. **07**

(b) Consider a resistive-load inverter with V_{DD} = 5V, k_n` = 20μA/V^2, V_{TO}= 0.8V, R_L = 200kΩ and W/L = 2. Calculate the critical voltages (V_{OL}, V_{OH}, V_{IL}, and V_{IH}) on the VTC and find the noise margins of the circuits. **07**

OR

Q.3 **(a)** Draw and explain the CMOS inverter. Find the V_{IL}, V_{IH} and V_{th} equation for the same. **07**

(b) Consider a CMOS inverter circuit with the following parameters: **07**

V_{DD} = 3.3 V,

For NMOS, $V_{TO, n}$ = 0.6 V, k_n=200 μ A/V^2

For PMOS, $V_{TO, p}$ = - 0.7 V, k_p=80 μ A/V^2

Calculate noise margin of the circuit considering k_R = 2.5

Q.4	**(a)**	Explain the behavioral of bistable elements	**07**
	(b)	Answer the following questions	
		1. Draw the circuit diagram of CMOS implementation of D-latch along with the simplified view. Also explain the timing diagram of it.	**03** **04**
		2. Explain voltage bootstrapping.	
		OR	
Q.4	**(a)**	Calculate the delay time for CMOS inverter during its high to low transition.	**07**
	(b)	Explain CMOS transmission gate (Pass gates) with different region.	**07**
Q.5	**(a)**	Explain with circuit two input CMOS NOR and NAND gate. Also derive threshold voltage for both.	**07**
	(b)	Answer the following questions	
		1. Realised following Boolean equation using CMOS transmission gates F=AB+A'C'+AB'C	**03**
		2. Draw Six-transistor CMOS transmission gate implementation of the XOR function	**02**
		3. Realised following Boolean function using CMOS. F=AB+C(D+E)	**02**
		OR	
Q.5	**(a)**	Explain basic principle of pass transistor with logic "1" transfer and logic "0" transfer. And plot the curve of output voltage in both the case.	**07**
	(b)	By taking suitable examples, discuss the ratioed and ratio-less dynamic logic circuits	**07**

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