Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

ME Semester –I Examination Feb. - 2012

Subject code: 712602N **Date: 13/02/2012**
Subject Name: CMOS Circuit Design-I
Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Compare and discuss Full scaling, General scaling and Fixed voltage scaling.	**07**
	(b)	Discuss any two second order effects.	**07**
Q.2	**(a)**	Draw common gate stage with direct and capacitive coupling at input. Also derive gain.	**07**
	(b)	Discuss carry bypass adder.	**07**
		OR	
	(b)	Compare Barrel Shifter and Logarithmic shifter.	**07**
Q.3	**(a)**	Derive voltage gain of source follower. Also draw the source follower using an NMOS transistor as current source.	**07**
	(b)	In source follower using an NMOS transistor as current source, M1 MOSFET acts as source follower and M2 MOSFET as current source. $(W/L)_1 = 20/0.5$, $I_1 = 200$ micro ampere, $V_{THO} = 0.6$ V, $2Ø_F = 0.7$ V, $\mu nCox = 50$ micro ampere/V^2, and $\gamma = 0.4$ V^2: (I) Calculate Vout for Vin =1.2 V. (II) Find the minimum value of $(W/L)_2$ for which M2 remains saturated.	**07**
		OR	
Q.3	**(a)**	Discuss Common Mode response for differential amplifier in detail.	**07**
	(b)	With which two important aspects of differential pairs, we can develop a versatile building block. Discuss Gilbert cell.	**07**
Q.4	**(a)**	Discuss Cascode current mirrors in brief.	**07**
	(b)	Discuss Small signal analysis of active current mirror.	**07**
		OR	
Q.4	**(a)**	List the performance parameter and draw simple op-amp topologies and discuss it in brief.	**07**
Q.4	**(b)**	Discuss following for power and speed trade-offs in data-path structures: (I) Using multiple supply voltage (II) Using multiple device threshold	**07**
Q.5	**(a)**	Describe following in CMOS inverter: (I) Switching Threshold (II) Noise Margin	**07**
	(b)	Discuss the array multiplier in partial product accumulation.	**07**
		OR	
Q.5	**(a)**	Draw and discuss Bode plot of loop gain for a one-pole and two-pole system.	**07**
	(b)	Draw high frequency model of a common-source stage and discuss the same.	**07**

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