Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

ME Semester –I Examination Feb. - 2012

Subject code: 714103N **Date: 17/02/2012**

Subject Name: Digital Signal Processor Architecture

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Consider the real-time DSP system as shown in Figure-1 and answer the following questions. Assume that ADC and DAC are ideal.

i. Let the input signal be $x_c(t) = \cos(3000\pi t)$ and there is no processing, i.e. $y[n] = x[n]$. Under what condition will $y_c(t) = x_c(t)$? **02**

ii. Consider the same input signal as above and suppose $y[n] = x^3[n]$. Under what condition will $y_c(t) = x_c^3(t)$? **05**

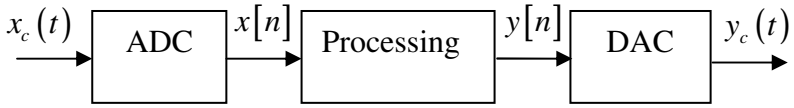

Figure-1

(b) Explain at least four advantages of DSP systems over analog systems. Also explain the role of analog circuits in DSP systems. **07**

Q.2 **(a)** Using FIR filter equation, explain the demands of DSP algorithms. How programmable digital signal processors meet these demands? **07**

(b) In a CD player, the sampling rate is 44.1 kHz, and each audio sample is quantized to 16 bits. If the CD player requires a 300-tap FIR filter, what kind of DSP processors has an adequate million-instructions-per-second (MIPS) rating to perform this task? What is the size of memory required to store up to 30 minutes of digitized stereo signal? **07**

OR

(b) List and explain finite-word length effects. **07**

Q.3 **(a)** Explain the differences between VLIW architecture and superscalar architecture. **07**

(b) Using block diagram, explain the operation of MAC unit in detail. List the techniques used to prevent overflow and underflow in MAC unit. **07**

OR

Q.3 **(a)** Compare RISC and CISC processors. **07**

(b) A non-pipeline system takes 100 ns to process a task. The same task can be processed in a 5-stage pipeline with the time delay of each segment in the pipeline is given as 20ns, 25ns, 30ns, 10ns, and 15ns. Determine the speed-up ratio of the pipeline for 10, 100, and 1000 tasks. What is the maximum speed-up that can be achieved? **07**

Q.4 **(a)** Explain various on-chip peripherals in TMS320C5X. **07**

(b) Explain the pipeline operation for following program involving only single-word single-cycle instructions: **07**

```
ADD    *+
SAMM   TREG0
MPY    *+
SQRA   *+, AR2
```

OR

Q.4 **(a)** Write TMS320C5X assembly language program to implement the sum of squared N consecutive samples expressed as $E_x = \sum_{i=0}^{N-1} x^2(i)$. Explain use of each instruction clearly. **07**

(b) List bits of status register 0 (ST0) of TMS3205X and their functions. **07**

Q.5 **(a)** List features of TMS320C6X processors. **07**

(b) Show hardware set up required to generate echo effect using DSK6713. Assuming one echo path, explain echo effect with block diagram and difference equation. Write a function in C language to implement an echo effect. Use following syntax for function: **07**

```
int echo (int input)
{
  /* write your code here */
}
```

OR

Q.5 **(a)** Using block diagram, explain 'C6000 McBSP operation. **07**

(b) List addressing modes supported by 'C6x and explain following instructions with suitable examples: **07**

(i) LDW .D1 *++A0[A4], A1

(ii) MVKH .S1 0A329123h, A1

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