

**GUJARAT TECHNOLOGICAL UNIVERSITY**  
**ME Semester –I Examination Feb. - 2012**

Subject code: 714201N

Date: 11/02/2012

Subject Name: Principles of VLSI Design

Time: 10.30 am – 01.00 pm

Total Marks: 70

**Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

- Q.1** (a) Draw and explain the VTC of Resistive Load Inverter. Derive the necessary equations for the same. **07**
- (b) Explain the following terms with respect to fabrication.
1. Vias. **04**
  2. LOCOS. **03**
  3. Layout Design Rules.
- Q.2** (a) What is Photoresist? List the different types of Photoresist materials and explain each in detail. **07**
- (b) Calculate the critical voltage  $V_{OL}$ ,  $V_{OH}$ ,  $V_{IL}$ ,  $V_{IH}$  and find the noise margin of the resistive-load inverter circuit with following parameters.  
 $V_{DD} = 5V$ ,  $V_{TO} = 0.8V$ ,  $W/L = 2$ ,  $k'_n = 20\mu A/V^2$ ,  $R_L = 200k\Omega$ . **07**
- OR**
- (b) Draw and explain CMOS SR latch based on NOR Gate. **07**
- Q.3** (a) Implement the following Boolean equation by using CMOS. Draw the stick diagram of the same by using Euler path.  
 $Y = [P(S+T)+QR]$  **07**
- (b) What is voltage bootstrapping? Explain Dynamic bootstrapping arrangement with necessary figures and equations. **07**
- OR**
- Q.3** (a) With the necessary wave forms and equations explain the following terms of typical Inverter. **07**
- (1)  $\tau_{PHL}$  and  $\tau_{PLH}$
  - (2)  $\tau_{rise}$  and  $\tau_{fall}$
- (b) Write down and explain the LEVEL 3 Model equations. **07**
- Q.4** (a) Explain the CMOS Ring Oscillator with necessary circuit and waveforms. **07**
- (b) Draw and explain the Y-chart. **07**
- OR**
- Q.4** (a) Write a short note on CMOS Transmission Gate. **07**
- (b) Draw and explain 4-bit x 4bit NOR-based ROM array. **07**
- Q.5** (a) Implement the clocked JK latch by using NAND gate only and explain the operation of the same in detail. **07**
- (b) With necessary steps explain the CMOS n-well process. **07**
- OR**
- Q.5** (a) Draw and explain the typical BiCMOS inverter circuit. **07**
- (b) Draw the stick diagram of following gates. **07**
- (1) NOR.
  - (2) NAND.

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