Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

ME Semester –III Examination Dec. - 2011

Subject code: 732604 **Date: 08/12/2011**
Subject Name: Low Power CMOS VLSI Circuit Design
Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What is Active Power dissipation? Discuss different components of Dynamic portion of the power dissipation in brief.	**07**
	(b)	Compare Conventional & RAMBUS DRAM architectures.	**07**
Q.2	**(a)**	List and Explain different techniques to achieve multiple threshold voltages in CMOS.	**07**
	(b)	Discuss the operation of 8 bit Carry Select Adders.	**07**
		OR	
	(b)	Explain with block diagram clocked sequential residue adder.	**07**
Q.3	**(a)**	Explain functioning of single SDDA cell and discuss how it can be extended as n-digit decimal adder.	**07**
	(b)	Discuss the different types of multiplier architectures in detail.	**07**
		OR	
Q.3	**(a)**	Explain 4:2 compressor and discuss its advantages over 3:2 compressors.	**07**
	(b)	Compare Drain-side programming and Source-Side Programming.	**07**
Q.4	**(a)**	Discuss different architectures of ROM for low power design.	**07**
	(b)	Explain the role of on-chip pulse generator in reducing active power in memories in detail.	**07**
		OR	
Q.4	**(a)**	Discuss the operation of Shared-BL SRAM cell and explain the cause of increased access time.	**07**
	(b)	Discuss the operation of CMOS differential to digital converter with circuit.	**07**
Q.5	**(a)**	Why do we use Back-Bias Generator? Explain Low voltage Back-Bias generator using Hybrid pumping scheme.	**07**
	(b)	Explain Pre-computation based optimization of sequential circuits for low power designs.	**07**
		OR	
Q.5	**(a)**	Discuss the major considerations in SRAM memory cell design.	**07**
	(b)	Compare XOR/XNOR gate implementations using PT-BiCMOS, TG-CMOS and CPL-CMOS.	**07**

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