Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER I - EXAMINATION – SUMMER 2017

Subject Code: 2710507 **Date:09/05/2017**

Subject Name: ASIC Design

Time: 02:30 pm to 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Answer the following **06**

i) List the major capabilities of VHDL along with the features that differentiate it from other hardware description languages.

ii) Describe different levels of abstraction in HDL

(b) Do as directed **08**

i) Declare entity for 8 bit Full Adder

ii) List nine values of std_logic

iii) Give one example each of concurrent and sequential statements

iv) Explain sensitivity list in process statement

Q.2 **(a)** Draw a flow chart indicating major steps involved in chip design using CAD tools. How is functional simulation different from timing simulation? **07**

(b) Write VHDL code using WHEN-ELSE statement for four bit comparator **07**

OR

(b) Write a behavioral VHDL code for 16 bit shift register with parallel loading and shift left-right control **07**

Q.3 **(a)** What is delta delay? Compare inertial and transport delay models with necessary examples **07**

(b) i) List various WAIT statements. **07**

ii) Using WAIT statement, write VHDL code for synchronous reset D flip flop

OR

Q.3 **(a)** Explain configuration and package declaration statements using necessary examples. **07**

(b) Discuss types of Finite State Machine (FSM) with appropriate example **07**

Q.4 **(a)** Give general structure of writing a test bench in VHDL. Write a test bench to generate D and clock inputs for D flip-flop. Assume VHDL code for D flip-flop is available. How do you limit simulation time? **07**

(b) Write VHDL code for **07**

(i) 4x1 MUX using with … select construct.

(ii) 1x4 DEMUX using when … else construct.

OR

Q.4 **(a)** Explain component declaration and component instantiation statement **07**

(b) Write VHDL code using structural model for a 4×1 MUX **07**

Q.5	**(a)**	Explain with a neat sketch the architecture of CLB's available in Xilinx FPGA.	**07**
	(b)	Discuss fuse and anti fuse technology of FPGA programming with appropriate diagram	**07**

OR

Q.5	**(a)**	Draw architecture or block diagram of one of the CPLD and explain its working	**07**
	(b)	Write short note on floor planning and placement	**07**

****