Seat No.: _____ Enrolment No._____

# GUJARAT TECHNOLOGICAL UNIVERSITY

**ME SEMESTER II EXAMINATION – SUMMER 2017**

**Subject Code: 2720314** **Date: 29/ 05 /2017**

**Subject Name: ADVANCE VLSI DESIGN**

**Time:02:30 PM to 05:00 PM** **Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

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|---|---|---|---|
| **Q.1** | | Consider Mealy Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognize the "1010" input bit sequence. Implement the state diagram for above and write Verilog code for it. | **14** |
| **Q.2** | **(a)** | Draw the timing diagram observed while simulating the design of $x^4$ implementation of Pipe line architecture in Xilinx ISE that shows all signals observed in simulation window and justifies functionality of the design. State throughput, latency and timing of your design with proper justification. | **07** |
| | **(b)** | Write the Verilog description of the module 3 bit magnitude-comparator using Dataflow. | **07** |
| | | OR | |
| | **(b)** | Write the Verilog program for find Factorial using Behaviour Modelling. | **07** |
| **Q.3** | **(a)** | Write the Verilog program for 4-bit Up-down counter using Behaviour Modelling. | **07** |
| | **(b)** | Write the Verilog program 4-bit Full Adder with look-ahead carry using structure Modelling. | **07** |
| | | OR | |
| **Q.3** | **(a)** | Write the Verilog program for data fetch from ROM using Behaviour Modelling. | **07** |
| | **(b)** | Write the Verilog program for Shift register using Behaviour Modelling. | **07** |
| **Q.4** | | Implement the function $Y = AX^4 + BX^3 + CX^2 + DX + E$ in verilog considering maximum time delay in the critical path of one 8 bit x 8 bit multiplier delayonly. Assume A, B, C, D,E, X, and Y of 8-bit. Draw implementation diagram of the same. What is the throughput and latency of your design?. | **14** |
| | | OR | |
| **Q.4** | **(a)** | Write a Verilog program for UDP of Negative Edge triggered D flip flop | **07** |
| | **(b)** | Write the Verilog program using Data flow modelling for 2 to 4 Decoder | **07** |
| **Q.5** | **(a)** | Write the verilog program and test bench for Binary to Gray(4-bit) code conversion | **07** |
| | **(b)** | What do you mean by metastability? With the help of timing diagram explain how setup and hold time of flip-flop cause metastability? | **07** |
| | | OR | |
| **Q.5** | **(a)** | Explain Register Balancing for timing in Architecting Speed. | **07** |
| | **(b)** | Implement logic function Y<= A'(B+C) using synchronous set & reset of D flip flop. Write Verilog code and implement diagram. | **07** |