Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME SEMESTER II EXAMINATION – SUMMER 2017

Subject Code: 2720511 **Date: 01/06/2017**

Subject Name: CMOS CIRCUIT DESIGN - I

Time:02:30 PM to 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the issue in Digital Integrated Circuit Design.	**07**
	(b)	Explain difference between single ended and differential operation.	**07**
Q.2	**(a)**	Describe the concept of static and dynamic CMOS circuit.	**07**
	(b)	Explain I/V characteristic of MOS.	**07**
		OR	
	(b)	Explain cascode current mirrors.	**07**
Q.3	**(a)**	Describe the basic MOS device physics and general consideration of MOS parameters. Describe the basic MOS device physics and general consideration of MOS parameters.	**07**
	(b)	Explain common source stage with diode connected load.	**07**
		OR	
Q.3	**(a)**	Explain in detail folded cascode amplifier.	**07**
	(b)	Describe the MOS small signal model.	**07**
Q.4	**(a)**	Explain compensation of two stage op amp and also explain other compensation techniques.	**07**
	(b)	Explain input output characteristic of CS configuration.	**07**
		OR	
Q.4	**(a)**	Explain 3 – stage ring oscillator.	**07**
	(b)	Describe the two stage op-amp and define slew rate & common mode feedback.	**07**
Q.5	**(a)**	Explain basic differential pair and analysis.	**07**
	(b)	Explain the following circuits (Any two) (i) Adder Circuits (ii) Multiplier (iii) Shifter	**07**
		OR	
Q.5	**(a)**	Explain the effect of technology scaling on the performance of CMOS inverter.	**07**
	(b)	Explain in short (i) Threshold voltage (ii) Noise margin. (iii) Circuit design levels.	**07**

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