Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME SEMESTER II EXAMINATION – SUMMER 2017

Subject Code: 2722602 Date: 25/05/2017

Subject Name: CMOS Circuit Design - II

Time:02:30 PM to 05:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks**

Q.1	**(a)**	Draw loop gain characteristics of simple charge pump PLL with and without R in series of C. Discuss the effect of R on stability of the circuit. Derive transfer functions of simple charge pump PLL with R in series of C.	**07**
	(b)	In a self-bias voltage reference circuit with resistor biasing, derive the dependence of output current on output resistance of each transistor in the circuit.	**07**
Q.2	**(a)**	How can we achieve temperature-independent output voltage in voltage reference circuit? Explain the principle of operation in detail with necessary derivation. Show that if one voltage source is taken as V_{BE}, then second voltage source should be 17.2 V_T.	**07**
	(b)	Explain with necessary diagrams and waveforms the issue observed in basic charge pump PLL due to finite capacitance seen at the drains of current sources. Suggest possible solution to this problem.	**07**
		OR	
	(b)	What will be the effect of unequal charging and discharging current in basic charge pump PLL on its operation? Explain with necessary waveforms.	**07**
Q.3	**(a)**	Show that NMOS and PMOS are poor conductors of '1' and '0', respectively. How can you transmit both levels with same accuracy? What are the precautions to be taken in this new structure of improved switch?	**07**
	(b)	Draw SC non-inverting amplifier circuit. What should be the sequence of switches to minimize charge injection effect? Justify your answer. Plot the output waveform taking into account the charge injection of all switches. Assume all switches are implemented with NMOS.	**07**
		OR	
Q.3	**(a)**	Draw multiply-by-two SC circuit. What should be sequence of operation of switches and why? Also draw its equivalent circuits for sampling and amplification phases.	**07**
	(b)	How can we realize resistor using combination of switches and capacitor? Explain working of basic SC integrator circuit (with two switches), discuss the problems associated with its accuracy and draw SC integrator circuit which solves problem of basic SC integrator circuit.	**07**
Q.4	**(a)**	Derive expression for final voltage on bit line capacitance when access	**07**

transistor gets ON in one-transistor-one-capacitor (1T1C) DRAM. Assume that bit line capacitance is initially charged to $V_{DD}/2$.

Calculate the change in the voltage across bit-line capacitance (100 fF) for a V_{DD} = 1V and DRAM capacitor 20 fF. Assume that the logic one is stored in DRAM cell.

(b) Explain the basic concept of using DSM (delta-sigma modulation) in sensing a flash memory. **07**

OR

Q.4 **(a)** Sketch a circuit for sensing resistive memory using a concept of DSM and derive expression of R_{mbit}. **07**

(b) Illustrate operation of sense amplifier having rail-to-rail input range. Discuss performance of the same from the point of view of kick-back noise, clock feed-through, power dissipation, and memory. **07**

Q.5 **(a)** What are the different performance parameters of voltage comparator? Explain in brief how would you measure each of them with diagrams and waveforms? **07**

(b) Define following terms related to DAC: 1. Dynamic range, 2. Quantization noise, 3. Signal-to-noise (SNR) ratio, and 4. Offset error. Derive expression for maximum value of SNR. **07**

OR

Q.5 **(a)** Explain the basic charge pump concept to generate positive voltage greater than V_{DD}. **07**

(b) Briefly discuss following parameters which play a critical role in the overall performance and design of LNA. **07**

1. Gain
2. Linearity
3. Bandwidth