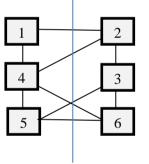
GUJARAT TECHNOLOGICAL UNIVERSITY ME - SEMESTER-II • EXAMINATION – SUMMER - 2017

Subject Code: 2722606Date: 30/05/2017Subject Name: Algorithms for VLSI Physical Design AutomationTime: 02:30 PM To 05:00 PMTotal Marks: 70

Instructions:

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.
- Q.1 (a) Discuss different layout styles with their advantage and disadvantage. 07
 - (b) Define (i) Rectangular dissection (ii) Slicing structure (iii) Skewed slicing tree (iv) Polish expression (v) Horizontal Constraint graph (vi) Channel intersection graph (vii) Trunk
- Q.2 (a) The Figure below is to be partitioned into two sub circuits. Apply Kernighan Lin heuristic to break the circuit into two equal size partitions so as to minimize the number of interconnections between partitions. Assume that all gates are of the same size and weight of all nets are 1. Initial partition is given in the figure.



	(b)	Explain Fiduccia-Mattheyses algorithm of circuit partitioning.	07
	(b)	OR Explain Simulated annealing algorithm of circuit partitioning.	07
Q.3	(a)	What are the objective parameters in placement of cells? How to calculate the total cost in placement?	07
	(b)	Solve the Cluster Growth algorithm for six cells with following netlist.	07
		N1={C1,C3,C4,C6}, N2={C1,C3,C5}, N3={C1,C2,C5}, N4={C1,C2,C4,C5}, N5={C2,C5,C6}, N6={C3,C6}	
		OR	
Q.3	(a)	Explain Properly triangulated planar graph and algorithm to construct it.	07
	(b)	Draw the slicing tree and floorplan of following polish expressions. (i) 12H34V56HVH (ii) 21H67V45VH3HV (iii) 21H43HV765HHV	07
Q.4	(a)	Describe force directed algorithm with ripple moves.	07
	(b)	Explain hadlock's algorithm.	07
		OR	
Q.4	(a)	Explain genetic algorithm.	07
	(b)	Describe line search algorithm of grid routing.	07
Q.5	(a)	Describe sequential global routing with steiner tree problem.	07
	(b)	Define procedure for greedy channel router.	07
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OR

- Q.5 (a) Explain Yoshimura and Kuh algorithm with example.(b) Discuss the optimization of standard cell layout.
