Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME– SEMESTER_II EXAMINATION – SUMMER - 2016

Subject Code: 2724202 **Date:26/05/2017**

Subject Name: Testing and Verification of VLSI Design

Time: **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the Testing Philosophy with suitable example.	**07**
	(b)	How Integration of Analog and Digital Device on one chi effect the testing.	**07**
Q.2	**(a)**	List down and discuss various approaches to reducing human-introduced errors.	**07**
	(b)	Define the following terms. 1. Design for Verification 2. Design Reuse 3. Verification Reuse	**07**
		OR	
	(b)	Discuss the fault detection by IDDQ test.	**07**
Q.3	**(a)**	Discuss the Failure mode analysis (FMA) with respect to role of Testing.	**07**
	(b)	Prove that verification is necessary evil.	**07**
		OR	
Q.3	**(a)**	Which are the two answer of the question “Is my design functionally correct?”. Explain the each answer w.r.t types of mistakes.	**07**
	(b)	Explain the ATPG with necessary block diagram.	**07**
Q.4	**(a)**	Compare testing and verification.	**07**
	(b)	Explain the following terms with respect to verification. 1. Testability 2. Controllability 3. Observability	**07**
		OR	
Q.4	**(a)**	List down the various type of testing depend on place and explain each in detail	**07**
	(b)	Once the device-under-test (DUT) has been mounted in the tester, which three things are needed to conduct the test? Explain each in detail.	**07**
Q.5	**(a)**	List down the various functional verification approach and discuss any two in detail.	**07**
	(b)	What is scan based testing? Explain it working in detail.	**07**
		OR	
Q.5	**(a)**	Draw and explain the functional model of memory.	**07**
	(b)	What is the delay test problem? Explain path delay test.	**07**

****