Seat No.: _____ **Enrolment No._____**

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2017

Subject code: 2724204 **Date: 30-05-2017**

Subject Name: HDL BASED DESIGN WITH PROGRAMMABLE LOGIC

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 (a) Do as Directed. 14

1. VHDL is a strongly typed language. (True/False)
2. Name any one system (Hw/Sw) description language. (SystemC)
3. Sensitivity list in the process statement is a type of Implicit Wait statement. (True/False)
4. Which VHDL construct is used for developing parameterized designs?
5. The 'next' statements skip the remaining statement in the _____ iteration of loop and execution starts from first statement of next iteration of loop.
   a. Previous **b.** Next **c.** Current (present) **d.** None of the above
6. Which among the following wait statement execution causes the enclosing process to suspend and then wait for an event to occur on the signals?
   a. Wait until Clk = '1' **b.** Wait on x,y,z
   c. Wait on clock until answer > 80 **d.** Wait for 12 ns
7. In Net-list language, the net-list is generated _____synthesizing VHDL code. (Before/After)
8. What is the usage of ALLIAS in VHDL?
9. What do you mean by resolution function in VHDL?
10. What are the components of a standard test-bench?
11. Explain the usage of (others => '_') statement in VHDL?
12. Mention the popular design approaches used in VLSI design.
13. Event driven simulator captures information on internal nodes also. – True/False
14. Which programmable hardware you will choose for implementing the design in which more flexibility is required – CPLD or FPGA? Why?

Q.2 (a) Explain what are the various levels of abstractions in VLSI design? 07

(b) 1. Discuss various types of delay models supported in VHDL? (3 Marks) 07

2. What do you mean by VLSI Design Quality? Discuss any four. (4 Marks)

OR

(b) What are the various modelling styles supported by HDLs? Discuss each one of them with suitable example. 07

Q.3 (a) Discuss pros and cons of Full Custom vs. Semi-custom VLSI design styles. 07

(b) 1. Draw and explain the architecture of an FPGA. (4 Marks) 07

2. Current FPGAs are used as SoC – Justify. (3 Marks)

OR

Q.3 (a) Write a VHDL description to implement 4-bit ALU with functions – Addition, Subtraction using 2's complement, Multiplication by 2, Division by 2. 07

(b) Explain following design constructs in reference to VHDL. 07

1. ARRAYS 2. RECORDS

Q.4 (a) What are the various logic implementation platforms available? Discuss in detail the selection criteria for the given application. 07

(b) Discuss the differences between Event-Driven and Cycle-Based Simulation. Explain the operation of Cycle based simulator in detail. 07

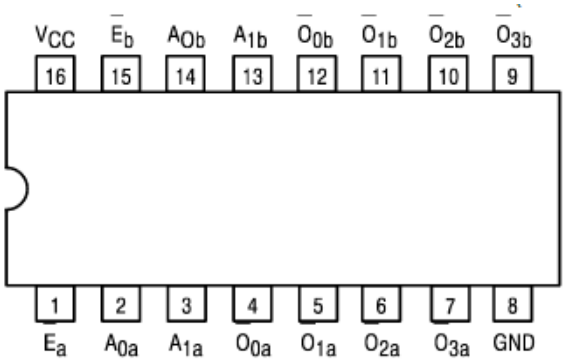
OR

Q.4 (a) Draw the Melay Machine state diagram for a sequence detector to detect an overlapping sequence of "110". Write the VHDL code for the same. 07

(b) What is synthesis? Explain following terms – 07

1. RTL Synthesis
2. High Level Synthesis
3. Gate Level Synthesis

Q.5 (a) The pin diagram and truth table for dual 2x4 line decode IC 74LS139 is shown below. Write the VHDL description for implementing the functionality of the chip. 07



TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

(b) 1. Discuss the main differences between Verilog and VHDL. (4 Marks) 07

2. What do you mean by High Level Synthesis? (3 Marks)

OR

Q.5 (a) Prepare the PLA table to realize following Boolean functions. Draw the structure of the programmed PLA to produce normal output. Count the total number of programmable links required in the PLA. 07

$$F_1 = \sum(0,2,4)$$
$$F_2 = \sum(0,1,3,7)$$
$$\overline{F_3} = \sum(5,7)$$

(b) Draw the RTL FOR below given VHDL code and rewrite the equivalent Verilog code for the same. 07

```
-----------------------------------------------------------------------
entity shift_reg is
port(   I:              in std_logic;
        clock:          in std_logic;
        shift:          in std_logic;
        Q:              out std_logic
);
end shift_reg;
-----------------------------------------------------------------------
architecture behv of shift_reg is

    -- initialize the declared signal
    signal S: std_logic_vector(2 downto 0):="111";

begin
    process(I, clock, shift, S)
    begin
        -- everything happens upon the clock changing
        if clock'event and clock='1' then
            if shift = '1' then
                S <= I & S(2 downto 1);
            end if;
        end if;
    end process;
    -- concurrent assignment
    Q <= S(0);
end behv;
-----------------------------------------------------------------------
```