

Seat No.: _____

Enrolment No. _____

GUJARAT TECHNOLOGICAL UNIVERSITY
M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2017

Subject code: 2724209

Date: 29-05-2017

Subject Name: VLSI Signal Processing

Time: 02:30 pm - 05:00 pm

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

Q1 (a) Define Following Terms. 07

- | | |
|---------------------|-----------------------------|
| 1. Iteration | 5. Critical Path |
| 2. Iteration Period | 6. Acyclic Precedence Graph |
| 3. Loop Bound | 7. Cutset |
| 4. Critical Loop | |

(b) Explain Fine-Grain Pipelining using FIR Filter. 07

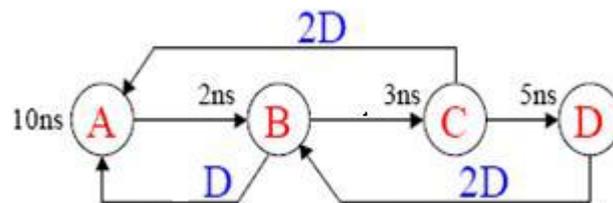
Q2 (a) Write a brief note on DSP Algorithms & its applications. 07

(b) Compare Pipelining & Parallel Processing for VLSI Signal Processing. 07

OR

(b) Write a note on look ahead computation in VLSI Signal Processing. 07

Q3 (a) Compute the iteration bound for DFG given below. 07



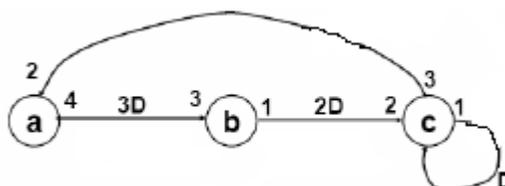
(b) Write a note on redundant number representation. 07

OR

Q3 (a) Define systolic design methodology. Compare it with other design methodologies.

(b) Explain operation of Parallel Multipliers.

Q4 (a) Transform below given MRDFG to SRDFG. 07

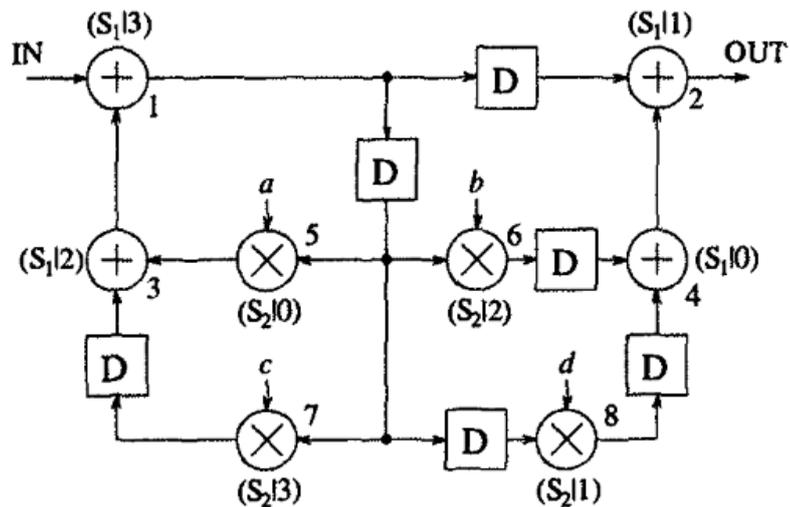


- (b) Draw a constraint graph for the below given system of inequalities. Decide whether the given system has a solution, and find the solution if exists using the Bellman-Ford algorithm. 07

$$\begin{aligned}
 r_1 - r_2 &\leq 1 \\
 r_3 - r_1 &\leq 3 \\
 r_4 - r_1 &\leq 2 \\
 r_4 - r_3 &\leq -1 \\
 r_3 - r_2 &\leq 1 \\
 r_5 - r_1 &\leq 2 \\
 r_3 - r_5 &\leq -1 \\
 r_4 - r_5 &\leq -2.
 \end{aligned}$$

OR

- Q4 (a) Retimed DFG for Biquad Filter is given. Redesign the filter with folding factor equal to 4. Use 1-stage pipelined adder and 2-stage pipelined multiplier. 07



- (b) Briefly discuss scaling and round off noise. 07

- Q5 (a) What are the different Power Reduction Techniques available? Discuss in brief. 07
 (b) What are the essential architectural features of DSP Processors? 07

OR

- Q5 (a) Briefly explain the unfolding algorithm. 07
 (b) Discuss Signal Transition Graphs. 07
