Seat No.: Enrolment	No
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Subject Code: 2725404 Subject Name: Mixed Signal Controllers

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER- IV EXAMINATION - SUMMER 2017

Date:25/05/2017

Time Instru		:30 PM to 05:00 PM Total Mark	ks: 70
	1. 2. 3.	Attempt all questions. Make suitable assumptions wherever necessary. Figures to the right indicate full marks. All the questions are related to MSP430 CPU.	
Q.1	(a)	Give justification for MSP430 series CPU having capabilities to achieve	07
	(b)	ultra low power designs. Describe the merits and demerits of DCO and Crystal for clock utilization.	07
Q.2	(a)	 Answer the following questions. 1) Describe the fail safe operation that can be achieved with the help of Oscillator Fault logic. 2) Using stack operations, explain how MSP430 CPU can switch from power down mode into active mode to serve interrupts. 	07
	(b)	Explain all the timer flags and their operations in MSP430 with their importance in application development. OR	07
	(b)	Describe the usage of Timer as a Counter in measuring the frequency of incoming signals.	07
Q.3	(a)	Describe the significance of Sample Timer in ADC. Explain the differences between Pulse Sample mode and Extended Sample mode.	07
	(b)	Explain the differences between "Single channel-single conversion mode" and "Repeat single channel mode" in ADC with importance of Trigger signal.	07
Q.3	(a)	OR An ADC12 is required to be configured for acquiring analog signal with sampling frequency of 1KHz. Describe the usage of Timer and ADC12 registers for generating this sampling frequency.	07
	(b)		07
Q.4	(a)	Describe the features of DAC12 in MSP430 with uniqueness associated with Group update.	07
	(b)	Answer the following questions regarding Watchdog Timer. 1) What is the significance of password byte when configuring watchdog timer register?	07
		2) What are the possible clock sources for Watchdog timer?3) How can you stop the watchdog timer?	
		4) Describe the interrupt activity in association with watchdog timer.	

OR

- **Q.4** (a) Describe the Hardware multiplier registers in MSP430 CPU with their **07** usage.
- Q.4 (b) Explain the block diagram of Comparator with signifying the application. 07
- Q.5 (a) Let there are two buffers 'A' and 'B' each with 10 elements. Buffer 'A' is treated as circular buffer to store incoming data and Buffer 'B' is holding coefficients of FIR filter. Write a C program to implement the convolution algorithm involving Multiply and Accumulate operation.
 - (b) Explain the requirement of DMA controller in application development. Of Describe the requirement of Single Transfer and Repeated Single Transfer mode individually with one application each.

OR

- Q.5 (a) List out at least three sources of Trigger for the DMA controller in 07 MSP430 CPU with an application in each case.
 - (b) Describe the requirements of DMA controller in digital signal processing **07** application to be implemented with MSP430 CPU.
