Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME – SEMESTER– III (NEW)- EXAMINATION – SUMMER-2017

Subject Code: 2734203 **Date:02/05/2017**

Subject Name: HIGH SPEED CMOS VLSI CIRCUIT

Time:02:30 pm to 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Compare various trade-offs in VLSI Circuit Design in detail and explain the importance of speed-power trade-off in VLSI Design.	**07**
	(b)	Discuss Parallel & Pipeline Architecture for High Speed CMOS VLSI Circuit.	**07**
Q.2	**(a)**	Explain in detail Impact of Scaling on High Speed VLSI Circuits.	**07**
	(b)	Explain the Elmore's model use for calculus of the delay in MOS circuits.	**07**
		OR	
	(b)	What is Mathematic Optimization? Compare different optimization algorithms.	**07**
Q.3	**(a)**	What is Circuit Optimization?	**07**
	(b)	Discuss in brief Roll of CAD Tool in Optimization of VLSI Design.	**07**
		OR	
Q.3	**(a)**	Discuss in brief importance of Simulated Annealing algorithm for optimization of VLSI Design.	**07**
	(b)	What are the different causes which fail the functionality of Chip?	**07**
Q.4	**(a)**	Explain the Complex model use for calculus of the delay in MOS circuits.	**07**
	(b)	Explain the Non-clocked Logic Circuit.	**07**
		OR	
Q.4	**(a)**	Explain the Different Styles of Single-Rail Domino Logic. Explain any one in detail.	**07**
	(b)	What is the importance of latching? Explain the performance of latching circuit with different mechanisms.	**07**
Q.5	**(a)**	Explain Static and Dynamic Latches.	**07**
	(b)	Explain the working of Pseudo Inverter latch.	**07**
		OR	
Q.5	**(a)**	Explain the working of Differential Cascode Voltage Switch (DCVS) Latch.	**07**
	(b)	What are the problems in controlling precharge circuit with single clock? Explain Cross Coupled Differential Output	**07**

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