Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY ME – SEMESTER– IV- EXAMINATION – SUMMER-2017

| | 0 | t Code: 2744202 Date: 03/05/20 t Name: Power Efficient VLSI Design | Date: 03/05/2017 | |
|-----|------------|---|------------------|--|
| Ti | me:0 | 2:30 PM TO 05:00PM Total Marks: ons: Attempt all questions. | 70 | |
| | 3. | Figures to the right indicate full marks. | | |
| Q.1 | (a) (b) | Discuss in detail with suitable diagram sources of power dissipation in CMOS. Explain the need of Power Efficient VLSI Design and explain in brief Power- Speed Trade-Off with suitable equations and examples. | 07 07 | |
| Q.2 | (a) (b) | What is Glitch? Discuss various techniques used for glitch reduction. Why n-well CMOS Process? Why not p-well CMOS Process? OR | 07 07 | |
| | (b) | Compare Power and Energy. What is more important Low Power Device or Low Energy Device? | 07 | |
| Q.3 | (a) (b) | Explain Self-Reverse Biasing. Derive mathematical formula to avoid negative tolerable skew and positive tolerable skew. | 07 07 | |
| | | OR | | |
| Q.3 | (a) (b) | Explain low dynamic power techniques. Explain Multi -V _T Technique. | 07 07 | |
| Q.4 | (a) (b) | Discuss Tolerable Skew v/s Zero Skew. Discuss data retention power sources for DRAM and SRAM. OR | 07 07 | |
| Q.4 | (a) | Discuss the effect of process variation on the performance of clock distribution | 07 | |
| | (b) | network. Compare SPICE simulation based power simulation v/s statistical based power estimation techniques. | 07 | |
| Q.5 | (a) | Discuss Monte Carlo Simulation Technique for power estimation with necessary expressions. | 07 | |
| | (b) | Discuss architectural level estimation technique. OR | 07 | |
| Q.5 | (a) | Discuss in brief the effect of transistor and gate sizing for Power Efficient VLSI Design. | 07 | |
| | (b) | Explain Power and Performance Management. | 07 | |
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1