Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER IV (NEW) – EXAMINATION – SUMMER - 2017

Subject Code: 2745402 **Date:03/05/2017**

Subject Name: CORTEX-M4 PROCESSOR ARCHITECTURE AND PROGRAMMING

Time:02:30PM-05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	1. What is the use of ICI/IT bit in XPSR register? 2. How to Enable FPU exception interrupts? 3. Give advantage of unaligned memory accesses compare to ARM Processor. 4. What is the use of PDDS bit in power control register? 5. What is a bit banding technique? 6. Explain the use of branch Prediction in pipeline. 7. Which three things need to use NVIC?	**07**
	(b)	What is SYSTICK timer? Explain each bit in SYSTICK control and status register?	**07**
Q.2	**(a)**	Write a short note on cortex-M series family.	**07**
	(b)	Explain the Programmer's model of cortex.	**07**
		OR	
	(b)	Explain NVIC and SCB registers for exception control.	**07**
Q.3	**(a)**	Explain the Low power modes of CORTEX.	**07**
	(b)	Explain 1) SADD 2) SHADD 3) LDMFD 4) LDREX with Example	**07**
		OR	
Q.3	**(a)**	How branch instructions are executed in CORTEX M4?	**07**
	(b)	Explain 1) BFC 2) LDMIA 3) MRS 4) MLA with Example.	**07**
Q.4	**(a)**	List the CMSIS intrinsic instruction and explain any two in detail.	**07**
	(b)	Explain with block diagram Cortex Microcontroller Software Interface standard (CMSIS).	**07**
		OR	
Q.4	**(a)**	Explain in Detail Memory Bit Band operation.	**07**
	(b)	Explain CMSIS usage, benefits and register core in detail.	**07**
Q.5	**(a)**	Explain the memory map of Cortex with all regions	**07**
	(b)	What is the difference between THUMB1 and THUMB2 Architecture?	**07**
		OR	
Q.5	**(a)**	Explain Instrumentation Macrocell and Embedded Trace Macrocell.	**07**
	(b)	Explain in detail Lazy stacking in Floating Point Unit.	**07**

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