Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– II EXAMINATION – SUMMER 2017

Subject Code: 3725203 **Date:29/05/2017**

Subject Name: Digital VLSI Design II Backend (Elective I)

Time:02:30 PM to 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the VLSI design cycle shortly with suitable diagram.	**07**
	(b)	Explain the Grid routing and discuss any one algorithm regarding grid routing.	**07**
Q.2	**(a)**	Explain the standard cell based design, Full custom design, and Gate array design.	**07**
	(b)	Explain the following terms: **1.** Hierarchy **2.** Modularity **3.** Regularity **4.** Locality.	**07**
		OR	
	(b)	List out the VLSI design challenges. Explain any two challenges.	**07**
Q.3	**(a)**	What are the steps involved in the floor planning stage and what is their importance?	**07**
	(b)	What is set up and hold time. How do they affect timing of a digital circuit with any equation?	**07**
		OR	
Q.3	**(a)**	What is the difference between wire delay and cell delay? How do they affect timing of the digital circuit?	**07**
	(b)	What are the steps involved in the placement stage and what s their importance?	**07**
Q.4	**(a)**	Explain the Generated clock and Gated clock.	**07**
	(b)	Explain the clock tree synthesis and issue of clock skew.	**07**
		OR	
Q.4	**(a)**	Explain the effects of clock tree optimization.	**07**
	(b)	Explain the inter clock delay balancing.	**07**
Q.5	**(a)**	Define terms: **1.** Moor's Law **2.** Non recurring cost **3.** yield **4.** Technology scaling	**07**
	(b)	How we can prevent the crosstalk in digital circuits?	**07**
		OR	
Q.5	**(a)**	Define terms: **1.** Congestion **2.** PNS **3.** PNA **4.** Wire sizing	**07**
	(b)	Explain the core routing based strategy.	**07**

****