Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME SEMESTER – I (OLD) EXAMINATION – SUMMER 2017

Subject Code: 710403N **Date:10/05/2017**

Subject Name: ASIC Design

Time:02:30 P.M. to 05:00 P.M. **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What are the different operators used in VHDL? Discuss with precedence.	**07**
	(b)	Explain Delta Delay, Transport Delay and Inertial Delay.	**07**
Q.2	**(a)**	Briefly explain the VLSI Design methodologies.	**07**
	(b)	Discuss Anti-fuse and static RAM programming Technology.	**07**
		OR	
	(b)	Write VHDL program for 4 – bit parallel adder.	**07**
Q.3	**(a)**	Use Switch – Case statement and write VHDL coding to realize 3X8 Decoder.	**07**
	(b)	Describe sequential and concurrent statements and also through some light on physical data types.	**07**
		OR	
Q.3	**(a)**	Use Case – When Statement and write VHDL coding to realize 4X1 MUX.	**07**
	(b)	Using with – select – when statement write VHDL program to have 4 – bit binary up and down counter with reset and preset facility.	**07**
Q.4	**(a)**	Discuss Timing Driven Placement.	**07**
	(b)	Describe the fish bone type of clock distribution scheme used for cell based ASIC.	**07**
		OR	
Q.4	**(a)**	Describe the Altera MAX Timing Model for local signals.	**07**
	(b)	Discuss how the wire – load tables are useful for delay measurement in floor planning?	**07**
Q.5	**(a)**	What do you mean by Design Entry, Place & Route?	**07**
	(b)	Write VHDL listing to realize following function:	**07**
		F = ABC + A'BD + AB'C'D + AD' +BC'	
		OR	
Q.5	**(a)**	Draw the basic block diagram of XC 9500 CPLD and Explain.	**07**
	(b)	Explain Xilinx 3000 Series logic cells with configuration memory cell.	**07**

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