

Seat No.: _____

Enrolment No. _____

GUJARAT TECHNOLOGICAL UNIVERSITY
ME SEMESTER III (OLD) EXAMINATION – SUMMER - 2017

Subject Code:730303

Date:04/05/2017

Subject Name: VLSI Design

Time:02:30 pm to 05:00 pm

Total Marks: 70

Instructions:

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks
4. Structural modeling programs must be accompanied by their respective diagrams.

Q.1 Consider Finite State Machine (FSM) with one input X and one output Z. The FSM asserts its output Z when it recognizes the input bit sequence "11001" at input X. Draw state machine diagram and write verilog code for this. (Hint: If input sequence is "111100110011..." then output will be "000000100010...") **14**

Q.2 (a) Write verilog code to design 7-segment decoder as a ROM, to display BCD numbers. **07**

(b) Write verilog code for 8-input encoder using case statement. Provide active low enable input for your design. **07**

OR

(b) Write verilog code for 8-bit universal shift register having shift left, shift right, parallel load and reset capabilities. **07**

Q.3 (a) Write verilog code for 3-input decoder having one active low and two active high enable inputs using behavioral modeling. **07**

(b) Write verilog code for T flip-flop having asynchronous set and preset using structural modeling. **07**

OR

Q.3 (a) Write verilog code for 4-bit shift-left register with a positive-edge clock, asynchronous clear, serial in and serial out. **07**

(b) Write verilog code for D flip-flop having asynchronous reset and synchronous preset using behavioral modeling. **07**

Q.4 (a) Define UDP of positive edge triggered T flip-flop having asynchronous set and reset inputs. **07**

(b) Define a function to multiply two 4-bit numbers A and B. The output is an 8-bit value. Invoke the function by using stimulus and display results. **07**

OR

Q.4 (a) Draw the circuit diagram of 32x1 multiplexer using 8x1 multiplexer and 2x4 decoder and/or basic gates. Write verilog code of the same. **07**

(b) Define a function to calculate the even parity of a 16-bit number and returns the value. Invoke the function by using stimulus and display the results. **07**

Q.5 (a) What is the difference between fine and coarse grained architecture of FPGA? Explain the architecture of FPGA with necessary diagram. **07**

(b) Write verilog code for the full subtractor using dataflow modeling and test all possible input combinations of the truth table using stimulus. **07**

OR

- Q.5** With the help of JK flip-flop design a synchronous counter that gives 0,1,4,6,7,0,1,... as an output sequence. Show all your design steps (not description). Write verilog codes of the counter and all the components used in your design using structural modeling style. Provide asynchronous reset in your design. Write stimulus to check functionality of your design and display the output of stimulus. **14**
