Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2013

Subject code: 1710412 Date: 05-06-2013

Subject Name: Digital VLSI Design

Time: 10.30 am – 01.00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Define following Terms in brief **07**

1. Regularity
2. Modularity
3. Locality
4. Positive Photoresist
5. Body Effect
6. Overlap Capacitance
7. Channel Stop Implant

(b) Explain CMOS fabrication process with necessary diagram **07**

Q.2 **(a)** What do you mean by MOSFET Scaling? Explain Constant-field Scaling and Constant-voltage Scaling in detail **07**

(b) Calculate the threshold voltage V_{TO} at V_{SB}= 0, for a polysilicon gate n-channel MOS transistor, with the following parameters: **07**
Substrate doping density $N_A=10^{16}cm^{-3}$,
polysilicon gate density $N_D=2 \times 10^{20}cm^{-3}$,
gate oxide thickness t_{ox}=500 Angstrom and
oxide interface fixed charge density $N_{ox}= 4 \times 10^{10}cm^{-2}$,
$\tilde{u}_F$(gate) = 0.55V.
Physical constants :
Thermal voltage =KT/q = 0.026 volt
Energy Gap of silicon(Si) =E_g = 1.12 eV
Intrinsic Carrier Concentration of silicon = $n_i=1.45 \times 10^{10}$ cm ï 3
Dielectric constant of vaccume = $\mathring{U}_o$ =8.85 x 10^{-14}F/cm
Dielectric constant of silicon = $\mathring{U}_{si}$ = 11.7 x $\mathring{U}_o$F/cm
Dielectric constant of silicon dioxide = $\mathring{U}_{ox}$ = 3.97 x $\mathring{U}_o$F/cm

OR

(b) Discuss procedure to measure data for experimental determination of the parameters k_n, V_{TO} and substrate bias coefficient. **07**

Q.3 **(a)** With neat sketch explain gradual channel approximation and derive the equation for drain current in linear region mode and saturation mode **07**

(b) Derive expressions for V_{IH} and V_{IL} for CMOS Inverter. **07**

OR

Q.3 **(a)** Draw two-input CMOS NOR gate and obtain expression for switching threshold voltage (v_{th}). Assume that both NMOS transistors are identical. Similarly, PMOS transistors are also identical. **07**

(b) Write a short note on short channel effects. **07**

Q.4 **(a)** Draw input and output waveform during high to low transition of output for a CMOS inverter and derive expression for $\acute{U}_{PHL}$ **07**

	(b)	Consider a resistive-load inverter circuit with V_{DD}= 5V, k_n'= 22µA/V^2, V_{T0}= 0.8 V, R_L= = 200 k, and W/L = 2. Calculate the critical voltages (V_{OL},V_{OH}, V_{IL},V_{IH}) on the VTC and find the noise margins of the circuit.	**07**
		OR	
Q.4	**(a)**	Discuss dynamic CMOS logic (precharge ï evaluate logic) with illustration of the cascading problem in dynamic CMOS logic.	**07**
	(b)	Explain three stage CMOS ring Oscillator in detail.	**07**
Q.5	**(a)**	Draw the circuit diagram and stick diagram of 3-input CMOS NAND gate.	**07**
	(b)	Explain CMOS transmission gate and design 4X1 Mux using transmission gate	**07**
		OR	
Q.5	**(a)**	Explain basic principles of pass transistor circuits.	**07**
	(b)	Draw and explain CMOS SR latch circuit	**07**

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