GUJARAT TECHNOLOGICAL UNIVERSITY M. E. - SEMESTER – I • EXAMINATION – SUMMER • 2013

M. E SEMESTER – I • EXAMINATION – SUMMER • 2013			
Subj	Subject code: 710403N Date: 13-06-2013		
Subject Name: ASIC Design			
Time: 10.30 am – 01.00 pm Total Marks: 70			
Instructions:			
1. Attempt all questions.			
		Make suitable assumptions wherever necessary.	
	3. Figures to the right indicate full marks.		
Q.1	(a)	What is ASIC? Draw and explain ASIC design flow.	07
C.	(b)	· ·	07
	. ,	2) List different abstraction level of Digital design. Also give difference	
		between top-bottom and bottom-top methodologies for digital design.	
Q.2	(a)		07
		differentiate it from other hardware description languages.	~ -
	(b)		07
		 Alias 2) Delta delay 3) Package 4) Generate statement Variable 6) signal 7) Wait statement 	
		OR	
	(b)		07
	(~)	between them.	0.
Q.3	(a)	Explain Behavioral Model of VHDL. Also Write VHDL code for 8 bit	07
		Magnitude Comparator using behavioral Model	
	(b)		07
		using any one Model of VHDL. Also write VHDL code for Master-slave JK flip flop	
		using Structural Model of VHDL in which this JK flip flop is used as a component. OR	
Q.3	(a)		07
2.0	(4)	VHDL Code for 1 X 4 DEMUX using	07
		1) WITH/SELECT/WHEN statement	
		2) Case statement	
	(b)		07
		Using: 1. If statement 2. When/else statement	
0.4	()		07
Q.4	(a)	Give difference between Moore FSM and Mealy FSM. Draw Moore FSM for BCD counter. Also write VHDL code for BCD Counter using Moore FSM	07
		model.	
	(b)		07
	(0)	OR	07
Q.4	(a)	Explain if-generate statement. Also write VHDL code for 4- bit counter using	07
		if-generate statement.	
Q.4	(b)	Write VHDL code for 1024 X 8 bit RAM with bidirectional in/out data bus.	07
Q.5	(a)		07
	(b)		07
		PLA, CPLD and FPGA. OR	
Q.5	(a)		07
V ••	(a) (b)	· ·	07
	()	**************************************	51
