Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – SUMMER • 2013

Subject code: 710412N **Date: 18-06-2013**

Subject Name: Digital VLSI Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the concept of Regularity, Modularity and Locality in detail	**07**
	(b)	Explain the need for LOCOS process, principal of LOCOS and LOCOS process with all necessary diagrams.	**07**
Q.2	**(a)**	Discuss procedure to measure data for experimental determination of the parameters k_n, V_{TO} and substrate bias coefficient.	**07**
	(b)	Define threshold voltage for MOS transistor. Describe the four component of threshold voltage.	**07**
		OR	
	(b)	Describe Accumulation, Depletion and Inversion process for the MOS system under external bias. Also derive the equation for maximum depletion region depth at the onset of surface inversion.	**07**
Q.3	**(a)**	What do you mean by MOSFET Scaling? Explain Constant-field Scaling and Constant-voltage Scaling in detail	**07**
	(b)	Draw and explain voltage transfer characteristic of CMOS inverter and discuss noise margin.	**07**
		OR	
Q.3	**(a)**	Draw two-input CMOS NAND gate and obtain expression for switching threshold voltage (v_{th}). Assume that both NMOS transistors are identical. Similarly, PMOS transistors are also identical.	**07**
	(b)	Write a short note on oxide related MOSFET capacitance.	**07**
Q.4	**(a)**	Define $\acute{U}_{PHL}$ and $\acute{U}_{PLH}$ for CMOS inverter. Derive $\acute{U}_{PHL}$ for CMOS Inverter	**07**
	(b)	What is CPL. Draw the circuit diagram of CPL NAND2 and CPL NOR2 gate and explain working.	**07**
		OR	
Q.4	**(a)**	Write short note on domino logic circuit	**07**
	(b)	Explain RC Delay model and Elmore delay model.	**07**
Q.5	**(a)**	Draw the circuit diagram and stick diagram of 2-input CMOS NOR gate.	**07**
	(b)	Explain CMOS transmission gate in detail.	**07**
		OR	
Q.5	**(a)**	Explain basic principles of pass transistor, using logic ñ1ò transfer event. How it is important in dynamic logic circuits.	**07**
	(b)	Draw and explain CMOS clocked JK latch circuit with waveform.	**07**

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