GUJARAT TECHNOLOGICAL UNIVERSITY
M. E. - SEMESTER – I • EXAMINATION – SUMMER • 2013

Subject code: 712602N   **Date: 04-06-2013**
Subject Name: CMOS Circuit Design-I
Time: 10.30 am – 01.00 pm   **Total Marks: 70**
Instructions:
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Discuss Technology scaling and its impact.	07
	(b)	What is the disadvantage of ripple carry adder? Discuss Carry óBypass Adders.	07
Q.2	**(a)**	Draw common source stage with diode connected load and derive voltage gain.	07
	(b)	Discuss Method I of Quantitative analysis of differential pair.	07
		OR	
	(b)	Explain dynamic dissipation due to Charging and Discharging Capacitances.	07
Q.3	**(a)**	Discuss Cascode stage and prove that the maximum voltage gain is roughly equal to the square of the intrinsic gain of the transistors.	07
	(b)	Derive the voltage gain of common gate stage.	07
		OR	
Q.3	**(a)**	Draw one bit Programmable Shifter and explain its operation. Also discuss Barrel Shifter.	07
	(b)	What is the advantage of Gilbert cell over simple differential pair? Discuss Gilbert cell.	07
Q.4	**(a)**	Explain Basic current mirrors in brief.	07
	(b)	Discuss Small signal analysis of active current mirror.	07
		OR	
Q.4	**(a)**	Briefly explain any two performance parameter of op-amps. Draw Cascode op-amps and discuss it.	07
Q.4	**(b)**	Explain following for power and speed trade-offs in data-path structures:	07
		(I) Reducing Switching Capacitance through Transistor Sizing	
		(II) Multiple supply inside a block	
Q.5	**(a)**	Draw high frequency equivalent circuit of a source follower stage and explain the same.	07
	(b)	Discuss the concept of tree and carry save multiplier.	07
		OR	
Q.5	**(a)**	Discuss Phase Margin in frequency compensation.	07
	(b)	Draw and explain high frequency model of a cascode stage.	07

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