Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – SUMMER • 2013

Subject code: 715205 **Date: 13-06-2013**

Subject Name: Advanced Computer Architecture

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1		Attempt the following questions:	
		(a) Explain the stored program model.	**5**
		(b) List and briefly define the possible states that define an instruction execution	**5**
		(c) What do mean by interrupt? Explain any one approach to deal with interrupt.	**4**
Q.2	**(a)**	Explain the principal of locality and define: spatial and temporal locality.	**07**
	(b)	Differentiate the RISC and CISC Architecture.	**07**
		OR	
	(b)	What is pipelining? Explain the various hazards that might be occurred during pipelining.	**07**
Q.3	**(a)**	Explain the cache size and mapping function parameter while cache design process.	**07**
	(b)	Explain PowerPC cache organization.	**07**
		OR	
Q.3	**(a)**	Explain Pentium-IV (4) cache organization.	**07**
	(b)	Explain the brief characteristics of following application specific processors: 1. Microcontroller 2. Network Controller 3. DSP	**07**
Q.4	**(a)**	Discuss the various addressing mode of instructions.	**07**
	(b)	Differentiate SRAM versus DRAM.	**07**
Q.4	**(a)**	What are the differences among EPROM, EEPROM and Flash Memory?	**07**
	(b)	Discuss the various disk performance parameters.	**07**
Q.5	**(a)**	Explain RAID.	**07**
	(b)	Explain SOC Architecture.	**07**
		OR	
Q.5	**(a)**	Explain the ARM processor in brief.	**07**
	(b)	Explain SPARC architecture in brief.	**07**

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