Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – III • EXAMINATION – SUMMER • 2013

Subject code: 730204 **Date: 15-05-2013**

Subject Name: Embedded Systems

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the various metrics that need to be optimized designing an embedded system.	**07**
	(b)	With a neat diagram explain the advance RAM architecture. Also explain how this is extended to improve the performance through synchronous DRAM.	**07**
Q.2	**(a)**	Explain the various events that take place when processors execute an instruction. Explain how pipelining improves the execution speed.	**07**
	(b)	Discuss the role of RTOS in Interrupt Handling and Task Scheduling.	**07**
		OR	
	(b)	Explain the reason why the systems with the conventional operating system fail to respond to the real time problems. Also explain how these are taken care in RTOS.	**07**
Q.3	**(a)**	What is "market window" and why is it so important for products to reach the market early in this window?	**07**
	(b)	Differentiate between (i) Single purpose and general purpose processors (ii) Synchronous communication and iso- synchronous communication	**07**
		OR	
Q.3	**(a)**	(I) Compose 1Kx 8 ROMs into a 2K× 16 ROM. (II) Sketch the internal design of a 4 × 3 RAM	**04** **03**
	(b)	Design a single purpose processor that outputs Fibonacci number up to n places. Start with a function computing the desired result, translate it into a state diagram, and sketch a probable datapath.	**07**
Q.4	**(a)**	What is multi-level bus architecture? Explain its need and also the to improve the processor performance by this architecture.	**07**
	(b)	Describe each tool that has enabled the elevation of software design and hardware design to higher abstraction levels.	**07**
		OR	
Q.4	**(a)**	Design a parallel I/O peripheral for the ISA bus. Provide : (i) A State Machine Description (ii) A Structural Description	**07**
	(b)	List three requirements of real-time systems and briefly describe each. Give examples of actual real-time systems to support your arguments.	**07**
Q.5	**(a)**	What is hardware/software co-simulation? What is a key method for speeding up such simulation?	**07**
	(b)	Explain Finite State Machine with example. Design the unit control process using a state machine.	**07**
		OR	

Q.5	**(a)**	List and define the three main IC technologies. What are the benefits of using each of the three different IC technologies?	**07**
	(b)	Compute the annual growth rate of (I) IC capacity (II) designer productivity.	**07**

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