Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – III • EXAMINATION – SUMMER • 2013

Subject code: 730303 **Date: 15-05-2013**

Subject Name: VLSI Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1		Consider Mealy Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognizes the "1110" input bit sequence. Implement the state diagram for above & write verilog code for it.	**14**
Q.2	**(a)**	Design a full subtractor circuit using full-adder and inverter. Write verilog modules for full-adder and inverter. Write verilog structural program for full subtractor using above modules.	**07**
	(b)	Explain the difference between net and register in verilog with appropriate example.	**07**
		OR	
	(b)	Explain gate delays in detail.	**07**
Q.3		Explain in detail configuration modes of FPGA.	**14**
		OR	
Q.3		Explain FPGA Spartan 3e family architecture with its components and neat diagram.	**14**
Q.4	**(a)**	Write a verilog program of 16-to-1 multiplexer using conditional operator.	**07**
	(b)	Compare ROM, PAL, PLA and PLD.	**07**
		OR	
Q.4	**(a)**	Write a verilog program of 3 to 8 decoder with enable input.	**07**
	(b)	How do sequential and parallel blocks vary in processing? Explain with the help of example.	**07**
Q.5		With the help of T flipflop, design 4-bit binary counter. Show all design steps. Write verilog program of the same using structural modeling style. Also write verilog program of all components used in your design.	**14**
		OR	
Q.5		Design a counter with a binary sequence 0,1,3,7,6,4 and repeat using T flipflop. Show all design steps. Write verilog program of the same using structural modeling style. Also write verilog program all components used in your design.	**14**

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