Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – III • EXAMINATION – SUMMER • 2013

Subject code: 732902 **Date: 15-05-2013**

Subject Name: VLSI Circuits and Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What are the basic building blocks of CMOS OPAMP? Draw them	**06**
	(b)	Compare for various aspects : (i) FPGA & ASIC and (ii) Voltage scaling & current Scaling	**08**
Q.2	**(a)**	Draw the Y –chart and explain the VLSI design process in detail.	**07**
	(b)	Draw and explain the different regions for (i) MOSFET V-I characteristics (ii) MOS C-V characteristics.	**07**
		OR	
	(b)	Define threshold voltage of a MOSFET. Also derive the equation for the same.	**07**
Q.3	**(a)**	Draw and explain the structure of depletion –type nMOS Transistor.	**07**
	(b)	Discuss MOSFET small signal model.	**07**
		OR	
Q.3	**(a)**	Realize CMOS-XOR gate. Stick diagram of CMOS - XOR gate is possible or not?	**06**
	(b)	(i) A logic gate has V_{OH} = 5 V, V_{OL} = 0.2 V, V_{IH} = 2.5 V, and V_{IL} = 0.8 V. Calculate the noise margins. (ii) In a resistive load inverter, load resistor is 5 k? , and the nMOS is modeled by a 200? resistor. Calculate the output voltage when input voltage is high.	**08**
Q.4	**(a)**	Explain NORA CMOS LOGIC circuit.	**06**
	(b)	Design a (i) Half adder circuit and (ii) Two – input NOR gate.	**08**
		OR	
Q.4	**(a)**	Draw the BiCMOS device structure and explain fabrication of same.	**06**
	(b)	Design (i) a SR latch circuit (ii) a Two-input XOR gate circuit.	**08**
		OR	
Q.5	**(a)**	Implement a two-input OR logic using BiCMOS.	**07**
	(b)	Write short note on: CPLD..	**07**
		OR	
Q.5	**(a)**	Draw the device structure of CMOS inverter. Show the different steps to fabricate a CMOS inverter.	**07**
	(b)	Write a short note on: Semiconductor memories.	**07**

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