Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – IV • EXAMINATION – SUMMER • 2013

Subject code: 740301 **Date: 14-05-2013**

Subject Name: Advanced VLSI Design

Time: 10.30 am – 01.00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Appropriate comment lines are must in your program**
4. **Figures to the right indicate full marks.**

Q.1 Implement the function $Y = AX^3 + BX^2 + CX + D$ in verilog considering maximum time delay in the critical path of one 8 bit x 8 bit multiplier delay only. Assume A, B, C, D, X, and Y of 8-bit. Draw implementation diagram of the same. What is the throughput and latency of your design? **14**

Q.2 (a) Implement the Boolean function Y = {C' (A + B) + Fô (D + E)] G' using minimum area as an optimization criteria. Consider that synchronous set and reset (both active high) D-flipflops are available as FDS element in the device. Write verilog code and draw implementation diagram of the same. What are the throughput, latency and timing of your design? **07**

(b) Implement the logic equation Y<= A' (B+C) using synchronous set and reset of D - flip-flop. Write verilog code and implementation diagram. **07**

OR

(b) What is the advantage and limitation of using dual edge triggered flip-flops? Write verilog code of dual edge triggered J-K flip-flop having synchronous reset. **07**

Q.3 In FPGA based system a clock source of 16 MHz is available. In this system, clocks of 1 MHz, 4 MHz and 8 MHz frequencies are also required, hence need to be generated internally by the system designer. Draw implementation diagram of the system and write verilog code for the same, which occupy minimum area in FPGA implementation. Justify how your system is meeting the required constraint. **14**

OR

Q.3 What is the cause of static hazard on an asynchronous reset? With the help of necessary waveforms explain static-1 hazard condition while generating active low reset signal given by reset <= AB + B'C. Give your suggestion to improve the design to prevent this hazard. **14**

Q.4 (a) Write in detail about clock trees and clock managers in FPGA with the help of necessary figures. **07**

(b) What do you meant by metastability? With the help of timing diagram explain it. A combinational circuit designed for Y<= (A+B) C has to pass from one clock domain (clock1) to another clock domain (clock2). Both of these clock domains are completely asynchronous. Write verilog program and draw implementation diagram to prevent metastable condition. **07**

OR

Q.4 (a) Write verilog code to implement following arithmetic (addition) operation. **10**

Y <= A + B if S1=0 and S0=0
Y <= B + C if S1=0 and S0=0
Y <= A + C if S1=1 and S0=X

Draw implementation diagram of the above with and without resource sharing option in synthesis tool. What is the advantage and limitation of using

resource sharing in this implementation?

	(b)	Draw implementation and timing diagram of the simulation of x^3 implemented using iterative scheme.	**04**
Q.5	**(a)**	With the help of necessary diagrams explain principles of CORDIC algorithm. Write verilog code of the same.	**07**
	(b)	When should we use if...else statement and case statement in implementation of priority encoder implementation? Justify their advantages and limitations with appropriate example.	**07**

OR

Q.5	**(a)**	With the help of figures explain different methods to optimize floor planning.	**07**
	(b)	With the help of verilog code and implementation diagram explain simple FSM and safe mode operated FSM.	**07**

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