Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2014

Subject code: 1710412 **Date: 23-06-2014**

Subject Name: Digital VLSI Design

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 Answer the following questions (Two marks each) **14**

(a) Discuss crosstalk and its implications.

(b) Compare static and dynamic circuit for size, power dissipation and speed of operation.

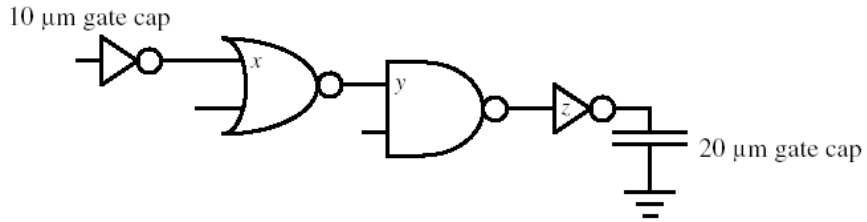
(c) Write equation for CMOS channel charge.

(d) Why CMOS is preferred compared to BJT in Digital VLSI design?

(e) Why CMOS flip-flops prefer non-overlapping clocks?

(f) What do you mean by Pseudo gate?

(g) For Circuit shown in figure below, find path logical effort and Path Electrical effort.



Q.2 **(a)** Show internal diagram of MOS transistor and explain calculation of gate capacitance. With diagram show variation of the gate capacitances as functions of gate-to-source voltage V_{GS} **07**

(b) Derive the drain current equation for MOSFET using Gradual Channel Approximation (GCA). **07**

OR

(b) State importance of Power-Delay Product and explain with necessary equations. **07**

Q.3 **(a)** With appropriate diagram discuss types of photoresists and their usage in lithography process. **07**

(b) Consider 5mm long, 0.32µm wide metal2 wire in 180nm process. The sheet resistance is 0.05Ω/□ and the capacitance is 0.2fF/µm. Estimate resistance and capacitance of the wire and construct a 3-segment π-model for the wire. A 10x unit-sized inverter drives a 2x inverter at the end of the 5mm wire. The gate capacitance is C = 2fF/µm and the effective resistance is R = 2.5KΩ Åµm for NMOS transistors. Neglect diffusion capacitance. Estimate the propagation delay using Elmore delay model. **07**

OR

Q.3 **(a)** With appropriate diagram explain how CMOS inverter is fabricated on plain substrate. **07**

	(b)	Sketch 2 input NOR gate with transistor widths chosen to achieve effective rise and fall resistance equal to a unit inverter. Compute the rising and falling propagation delays in terms of R and C of the NOR gate driving h identical NOR gates using Elmore delay model. If C = 2fF/µm and R = 2.5KΩ Åµm in a 180nm process, what is the delay of fanout-of-4 NOR gate?	**07**
Q.4	**(a)**	Derive critical voltages for CMOS inverter and find ratio of W/L for symmetrical inverter.	**07**
	(b)	Draw and compare 1-bit full adder circuit using CMOS compound gate and CMOS transmission gate. Illustrate which mechanism will use less number of transistors.	**07**
		OR	
Q.4	**(a)**	For depletion load inverter circuit, discuss noise margin with transfer characteristic.	**07**
	(b)	Draw MOS transistor level schematic and explain operation of D Latch as well D Flip-flop with waveforms.	**07**
Q.5	**(a)**	Explain concept of precharge and evaluate for dynamic logic circuit.	**07**
	(b)	What is feature size and λ? Explain Layout design rules in terms of λ.	**07**
		OR	
Q.5	**(a)**	Write short note on NORA CMOS logic.	**07**
	(b)	Draw Circuit diagram and stick diagram for following boolean function	**07**

(i) $Y = \overline{AB + C}$

(ii) $Y = \overline{ABC}$

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