Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2014

Subject code: 1722602 **Date: 18-06-2014**

Subject Name: CMOS Circuit Design - II

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	How can we realize resistor using combination of switches and capacitor? Explain working of basic SC integrator circuit (with two switches), discuss the problems associated with its accuracy and draw SC integrator circuit which solves problem of basic SC integrator circuit.	**07**
	(b)	Explain the working of SC non-inverting amplifier and how the sampling instant depends upon switching off of switch in the feedback path.	**07**
Q.2	**(a)**	Draw loop gain characteristics of simple charge pump PLL with and without R in series of C. Discuss the effect of R on stability of the circuit. Derive transfer functions of simple charge pump PLL with R in series of C.	**07**
	(b)	What will be the effect of unequal charging and discharging current in basic charge pump PLL on its operation? Explain with necessary waveforms.	**07**
		OR	
	(b)	Explain the effect of dead zone in charge pump circuit. How can you avoid it? Explain with necessary waveforms.	**07**
Q.3	**(a)**	In a self-bias voltage reference circuit with resistor biasing, derive the dependence of output current on output resistance of each transistor in the circuit.	**07**
	(b)	Draw and explain working of a circuit to generate PTAT current.	**07**
		OR	
Q.3	**(a)**	How can we achieve temperature-independent output voltage in voltage reference circuit? Explain the principle of operation in detail with necessary derivation. Show that if one voltage source is taken as V_{BE}, then second voltage source should be 17.2 V_T.	**07**
	(b)	Determine the small-signal output impedance of the bandgap reference circuit shown in Fig.1 and examine its behavior with frequency.	**07**
Q.4	**(a)**	Compare open-array and folded-array organization architectures of memory chip. Draw necessary schematics for both of them.	**07**
	(b)	How does implementation of comparator different compared to that of operational amplifier? Draw the circuit schematic of basic comparator and explain its working.	**07**
		OR	
Q.4	**(a)**	What is the need of sense amplifier in reading data from memory cell? Draw circuit diagram of clocked sense amplifier and explain its working. List out various performance parameters of sense amplifier.	**07**

	(b)	Explain the basic charge pump concept to generate negative voltage with a magnitude greater than V_{DD}.	**07**
Q.5	**(a)**	What is the need of buffered opamps? What are the different approaches to design buffered op-amp? Discuss one of them.	**07**
	(b)	Discuss different performance parameters of DAC as well as various sources of error affecting the output in DAC.	**07**

OR

Q.5	**(a)**	What are the different approaches to increase gain bandwidth product of the op-amp? Explain current feedback op-amp approach.	**07**
	(b)	Describe the operation of serial ADC with block diagram.	**07**

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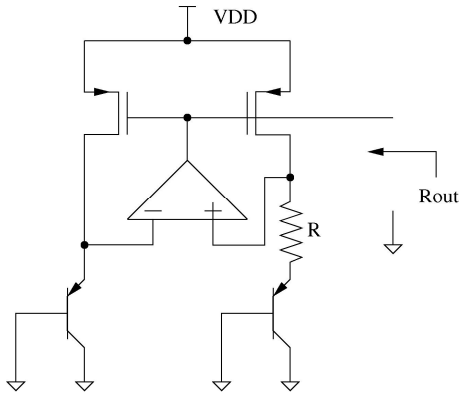

Fig. 1: Q:3 (b) OR