Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2014

Subject code: 1722606 Date: 01-07-2014

Subject Name: Algorithms for VLSI Physical Design Automation

Time: 02:30 pm - 05:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Discuss Programmable Logic Arrays. **07**

(b) Do as Directed: **07**

1. Compare Kernighan-Lin algorithm and Fiduccia-Mattheyses algorithm.
2. Discuss variations of Kernighan-Lin Algorithm

Q.2 **(a)** Consider the netlist given below: **07**

0 1 4 5 1 6 7 0 4 9 0 0

2 3 5 3 5 2 6 8 9 8 7 9

Find Zone table, Zone representation and VCG for channel routing problem.

(b) Explain Lee algorithm with Filling and Retrace. Briefly discuss its limitation. **07**

OR

(b) Explain the following: **07**

(1) Steiner tree
(2) Rentôs Rule
(3) Artificial Neural network
(4) Sea of Gates
(5) HVH model for channel routing
(6) Escape line in Hightowerôs Algorithm
(7) Behavioural level layout generation

Q.3 **(a)** Discuss simulated annealing algorithm for placement. **07**

(b) Discuss Graph representations of floorplan in detail. **07**

OR

Q.3 **(a)** Discuss Global routing by maze running. **07**

(b) Explain Headlock algorithm for grid routing **07**

Q.4 **(a)** Compare Unconstrained left edge algorithm and constrained left edge algorithm in detail. **07**

(b) Explain any one algorithm proposed by Yoshimura and Kuh. **07**

OR

Q.4 **(a)** Describe any three methods to estimate wirelength. **07**

Q.4 **(b)** Explain conversion algorithm for Global routing. **07**

Q.5 **(a)** Discuss Cluster growth algorithm for Floorplanning in brief. **07**

(b) Briefly explain: **07**

1. PLA personality
2. PLA Folding

OR

Q.5 **(a)** What is the problem with constrained left-edge algorithm? Discuss Dogleg algorithm. **07**

(b) Explain genetic algorithm for placement. **07**

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