Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2014

Subject code: 1722607 **Date: 01-07-2014**

Subject Name: VLSI Signal Processing

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

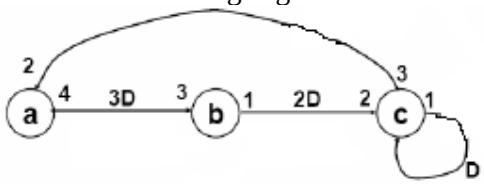
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 **(a)** Compare BD, DFG, and SFG representation for DSP Algorithm. **07**

(b) Draw Transposed SFG & Data Broadcast Structure of 3 Tap FIR Filter. **07**

Q.2 **(a)** Why use Parallel Processing when Pipeline Processing can be used equally well? Briefly explain with example. **07**

(b) Transform MRDFG to SRDFG of following Fig. **07**



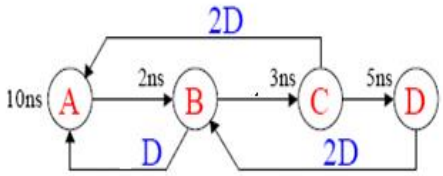
OR

(b) Explain Fine-Grain Pipelining using FIR Filter. **07**

Q.3 **(a)** Define Following. **07**

1. Iteration 2. Iteration Period 3. Loop Bound 4. Critical Loop 5. Cutset

(b) Compute the iteration bound for following Fig. **07**



OR

Q.3 **(a)** Write a brief note on DSP Algorithms. **07**

(b) Compare Pipelining & Parallel Processing for VSP. **07**

Q.4 **(a)** Define systolic design methodology. Compare it with other design methodology. **07**

(b) Write a note on fast convolution. **07**

OR

Q.4 **(a)** Briefly discuss the strength reduction in parallel FIR filters. **07**

(b) Write a note on look ahead computation. **07**

Q.5 **(a)** Briefly discuss scaling and round off noise. **07**

(b) Explain bit level arithmetic architecture. **07**

OR

Q.5 **(a)** Write a note on redundant number representation. **07**

(b) Discuss DSP applications. **07**

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