Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2014

Subject code: 1724201 **Date: 16-06-2014**

Subject Name: Power Efficient VLSI Design

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain Tolerable Skew v/s Zero Skew.	**07**
	(b)	A 32 bit off-chip bus operating at 5V and 66MHz clock rate is driving capacitance of 25pF/bit. Each bit is estimated to have a toggling probability of 0.25 at each cycle. What is power dissipation in operating the bus?	**07**
Q.2	**(a)**	Explain the need of power efficient VLSI Design. Discuss in detail Static Power Dissipation and Dynamic Power Dissipation in detail.	**07**
	(b)	Explain with example Power and Performance Management.	**07**
		OR	
	(b)	Explain Multi -V_T Technique.	**07**
Q.3	**(a)**	Discuss SRB Techniques for static power reduction.	**07**
	(b)	Explain in detail different clock distribution network.	**07**
		OR	
Q.3	**(a)**	Discuss in detail Parallel and Pipelining architecture methodology used for low power design.	**07**
	(b)	Discuss various sources of power dissipation in DRAM and SRAM.	**07**
Q.4	**(a)**	What is the significance of Switching Activity Reduction? Explain various technique used for the same in order to reduce power dissipation.	**07**
	(b)	The Chip size of a CPU is 15 mm x 25mm with clock frequency of 300MHz operating at 3.3V. The length of the clock routing is estimated to be twice the circumference of the chip. Assume that the clock signal is routed on a metal layer with width of 1.2 µm and the parasitic capacitance of the metal layer is 1fF/µm^2. What is the power dissipation of the clock signal?	**07**
		OR	
Q.4	**(a)**	Explain Twin Tub Process? Why high concentration of n-well is required?	**07**
	(b)	Discuss the significance of N-well process compared to P-Well CMOS Process.	**07**
Q.5	**(a)**	Compare Single Driver v/s Distributed Buffer scheme.	**07**
	(b)	Compare SPICE simulation v/s Statistical based power estimation techniques.	**07**
		OR	
Q.5	**(a)**	Derive mathematical expression to avoid negative tolerable skew and positive tolerable skew.	**07**
	(b)	Discuss Monte Carlo Simulation Technique for power estimation with necessary expressions.	**07**

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