Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2014

Subject code: 1724205 **Date: 23-06-2014**

Subject Name: Analog and Mixed Signal VLSI Design

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain basic of MOS model in Details.	**07**
	(b)	What is Analog and Mixed Signal VLSI, Give some examples of it mixed signal Design.	**07**
Q.2	**(a)**	Explain MOSFET-Only Voltage Divider.	**07**
	(b)	Using the small signal diagram derive the voltage gain and -3dB frequency of Active pMOS load inverter	**07**
		OR	
	(b)	What are the main Analog issues in CMOS Technology?	**07**
Q.3	**(a)**	Explain Diode Reference Self Biasing.	**07**
	(b)	Discuss layout techniques for improving matching of the device used as current mirror.	**07**
		OR	
Q.3	**(a)**	Discuss Phased Frequency Detector in details.	**07**
	(b)	Explain Wilson Current Mirror.	**07**
Q.4	**(a)**	Draw small signal equivalent of a case code amplifier and derive small signal gain and Rout formula for the circuit.	**07**
	(b)	What is the difference between PLL and DPLL? What is the need of a ñPhase detectorò in a DPLL?	**07**
		OR	
Q.4	**(a)**	Draw the block diagram of Random Access Memory. Also discuss DRAM and SRAM memory cell.	**07**
	(b)	What care must be taken while drawing a layout? Why analog matching is important in analog design? Discuss concept of device folding used for layout in Analog Design.	**07**
Q.5	**(a)**	In 3bit DAC if Vref = 2V, then find the value of LSB, MSB and respective analog values for input digital values.	**07**
	(b)	Explain ADC in detail with one example.	**07**
		OR	
Q.5	**(a)**	Define Following Specification of ADC (i)Missing Codes (ii) Offset and Gain Errors (iii) INL (iv) DNL (v) SNR	**07**
	(b)	Explain in detail R-2R DAC Architecture.	**07**

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