Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2014

Subject code: 2725203 **Date: 20-06-2014**

Subject Name: Digital VLSI Design-II Backend

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Draw the VLSI design flow with indicating verification at different stages of the design flow	**07**
	(b)	Discuss methodology of Physical Cycle Design.	**07**
Q.2	**(a)**	Write the floor planning goals and objectives. What is logic partitioning and physical Partitioning? What are partitioning algorithm.	**07**
	(b)	Discuss Clock Tree Synthesis (CTS) and its goals.	**07**
		OR	
	(b)	Explain the timing driven and congestion driven placement.	**07**
Q.3	**(a)**	What are the Goals and objectives of routing? Classify the routing Categories. Discuss the different area routing procedure with suitable examples	**07**
	(b)	Discuss Interconnect Delay Models	**07**
		OR	
Q.3	**(a)**	Discuss Global Route for congestion map.	**07**
	(b)	Discuss PNA(Power Network Analysis)	**07**
Q.4	**(a)**	What are goals and objectives of placement? What are the placement algorithms?	**07**
	(b)	Discuss Grid Based Routing System.	**07**
		OR	
Q.4	**(a)**	What do you mean by physical verification? Discuss several physical verification steps.	**07**
	(b)	What do you mean by Design Rules Check (DRC)? Discuss different design rules with examples?	**07**
Q.5	**(a)**	Discuss Crosstalk ï Induced Delay	**07**
	(b)	Discuss Effects of tree synthesis	**07**
		OR	
Q.5	**(a)**	Discuss Crosstalk ï Induced Noise	**07**
	(b)	Discuss PNS(Power Network Synthesis)	**07**

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