Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – II • EXAMINATION – SUMMER • 2014

Subject code: 2725205 **Date: 23-06-2014**

Subject Name: System On Chip Architecture

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	(a)	What performance bottleneck can typically arise when CPU-intensive software is run on a model of a complete System On Chip (SoC)? How can this be avoided and at what cost to modeling accuracy?	07
	(b)	Explain SoC design flow. Also explain difference in the flow if done for FPGA based SoC flow.	07
Q.2	(a)	How is chip level timing analysis done for SoCs? What are various timing parameters needed to perform timing closure?	07
	(b)	Design SoC for networking world. Note: The SoC will be used at datacenter servers	07
		OR	
	(b)	Technology predictions are that chip transistor count can continue to grow provided a lower percentage of the chip is in use at any one time. How can large parts of application programs be implemented in custom hardware and would this match technology trends?	07
Q.3	(a)	Case study: The inner loop of an application program, to be implemented within a SoC, performs a lot of bit-intensive operations on 64-bit numbers. Two of the operations are counting the number of ones and reversing the bits. What design considerations should be taken into account when deciding whether to speed up the implementation of these operations using custom hardware?	07
	(b)	Summarise each of the following three means of coupling custom hardware to a processor sub-system within a SoC: (i) implemented as a custom instruction (ii) implemented in a peripheral controlled using programmed I/O (iii) implemented in an autonomous bus master	07
		OR	
Q.3	(a)	What is Network on Chip (NoC)? What are different ways to implement NoC on a SoC?	07
	(b)	Comment of clocking structures used in SoCs. How can one achieve gated clocks in FPGA based SoC flow? How to achieve data synchronization in multiple clock design where all clocks are unrelated?	07
Q.4	(a)	Explain how clock skew affects setup and hold requirements of a flip-flop. How does designer account for duty cycle and jitter in timing analysis?	07
	(b)	What are the key factors in deciding a SoC based design Vs ASIC based design or pure FPGA based design?	07
		OR	
Q.4	(a)	What is synchronizer? How to calculate MTBF for a synchronizer?	07

(b) Case study: A particular design requires double precision floating point arithmetic. While selecting a SoC, designer has two options viz. 07

i) Select a SoC which has floating point ALU with associated instructions defined in the ISA.

ii) Select a SoC which has floating point ALU as co-processor with associated co-processor access instructions.

What would be the most effective choice and why?

Q.5 (a) A certain SoC has out of order execution architecture. Comment on performance impact it may have compared to in-order execution architecture. 07

(b) A SoC consumes about 50W power at 1.2V. To provide regulated 1.2V power source to this SoC, what would be the appropriate choice of regulator type. (Considering Linear and switching regulators). Explain factors to support your choice. 07

OR

Q.5 (a) What do you understand by the term ñDeep Sub Micron (DSM)ò and how it may affect reliability of chip functionality of a high speed SoC? 07

(b) What is Transaction level modeling (TLM) and explain TLM with SystemC. 07

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