Seat No.: _____ *Enrolment No._____*

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – I • EXAMINATION – SUMMER • 2014

Subject code: 714103N **Date: 19-06-2014**

Subject Name: Digital Signal Processor Architecture

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain the role of anti-aliasing filter and reconstruction filter in the design of a DSP system.	**07**
	(b)	What is the difference between normal shifter and barrel shifter? Explain 4-bit shift right barrel shifter using necessary diagram.	**07**
Q.2	**(a)**	List various special addressing modes found in P-DSPs and briefly explain any two of them.	**07**
	(b)	We want to implement the linear convolution of entire 10,000-point sequence with 100 points long FIR impulse response. The convolution is to be implemented by using DFTs and inverse DFTs of length 256. If the overlap-add method is used, what is the minimum number of DFTs and IDFTs needed for this task? Justify your answer.	**07**
		OR	
	(b)	Explain overlap-add method of block convolution using DFT.	**07**
Q.3	**(a)**	Consider a non-pipelined machine with six execution stages of lengths 50 ns, 50 ns, 60 ns, 60 ns, 50 ns, 50 ns. Find the instruction latency and time required to execute 100 instructions. Suppose we introduce pipelining on this machine. Assume that when introducing pipelining, the clock skew adds 5 ns of overhead to each execution stage. Find the instruction latency and time required to execute 100 instructions after pipelining. Also find the speedup obtained from pipeline for execution of 100 instructions.	**07**
	(b)	Explain how a higher throughput is obtained using the VLIW architecture.	**07**
		OR	
Q.3	**(a)**	Explain the operation of TDM serial ports in P-DSPs.	**07**
	(b)	Explain stream processing and block processing methods of real-time computation.	**07**
Q.4	**(a)**	Explain internal architecture of TMS320C5X using block diargram.	**07**
	(b)	Explain SACB, SACL and SACH instructions of TMS320C5X.	**07**
		OR	
Q.4	**(a)**	List and explain four phases of TMS320C5X pipeline.	**07**
	(b)	Explain LST and SST instructions of TMS320C5X.	**07**
Q.5	**(a)**	Explain address generation options present in linear addressing mode of ó C6X.	**07**
	(b)	List the features of McBSP.	**07**
		OR	
Q.5	**(a)**	What is register file cross path? Explain register file cross path of TMS320C6X.	**07**
	(b)	Explain MVKL and MVKH instructions of TMS320C6X.	**07**

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