Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

M. E. - SEMESTER – III • EXAMINATION – SUMMER • 2014

Subject code: 732902 **Date: 05-06-2014**

Subject Name: VLSI Circuits and Design

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1 Do as directed: (7 x 02 Marks each) **14**

1. What do you mean by hierarchal abstraction?
2. Justify statements.ò PMOS is usually constructed on p type substrate.ò
3. Define the following: Observability and Failure in Time.
4. Draw the flow diagram of typical VLSI design flow.
5. What do you mean by hot electron effect?
6. Draw small signal model of nMOS diode.
7. Enlist disadvantages of BiCMOS.

Q.2 **(a)** State criteria in designing semiconductor memories. Discuss DRAM in detail. **07**

(b) Explain the following process for VLSI fabrication with sketches: (i) Oxidation (ii) Photo-lithography. **07**

OR

(b) What do you mean by DFT (design for testability)? Discuss different DFT methodologies. **07**

Q.3 **(a)** Derive an equation for saturated drain current considering channel length modulation for MOS transistor. **07**

(b) What do you meant by MOSFET scaling? Discuss constant-field scaling and constant voltage scaling? **07**

OR

Q.3 **(a)** Define threshold voltage of a MOSFET. Also derive an equation of threshold voltage of a MOSFET. **07**

(b) Discuss short channel effects in detail. **07**

Q.4 **(a)** Discuss transfer of logic 1 through an nMOS transistor. **07**

(b) Design a (i) CMOS NOT Gate and (ii) Two ï input NAND gate. **07**

OR

Q.4 **(a)** Along with frequency response, discuss the CMOS amplifier **07**

(b) Realize the optimized CMOS logic circuit for (i) a half-adder circuit and (ii) a tri-state buffer. **07**

Q.5 **(a)** Implement a two ï input NOR logic using BiCMOS. **07**

(b) Write short note on :ASIC **07**

OR

Q.5 **(a)** Compare FPGA and CPLD for various aspects. **07**

(b) Design a BiCMOS inverter logic circuit. State its advantages. **07**

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