Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–IV • EXAMINATION– SUMMER • 2014

Subject Code: 740301 **Date: 04-06-2014**

Subject Name: Advanced VLSI Design

Time: 02:30 pm - 05:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Explain how critical paths can be minimized by reorder paths.	**07**
	(b)	Explain the impact of resource sharing on area.	**07**
Q.2	**(a)**	Explain software/hardware codesign in brief.	**07**
	(b)	Explain double flopping method for minimizing the probability of metastability.	**07**
		OR	
	(b)	Explain the problems with fully Asynchronous Resets.	**07**
Q.3	**(a)**	Explain clock skew and how it can be managed in power architecting.	**07**
	(b)	How internally generated resets cause static hazard? Explain with its remedy.	**07**
		OR	
Q.3		Explain trade-offs between priority and parallel structures in creating efficient decision tree.	**14**
Q.4	**(a)**	Explain inferred latches in FPGA designs.	**07**
	(b)	Explain the effect of reset on register balancing.	**07**
		OR	
Q.4	**(a)**	Explain Asynchronous Assertion, Synchronous deassertion technique for reset pin	**07**
	(b)	Explain High-throughput architectures in Architecting speed.	**07**
Q.5		Explain in detail speed versus area in Synthesis optimization.	**14**
		OR	
Q.5	**(a)**	How power can be minimized using input control?	**07**
	(b)	Define Metastability and describe Metastability caused by timing violation.	**07**

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