Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– II (Old course)• REMEDIAL EXAMINATION – SUMMER 2015

Subject Code: 1710412 **Date:18/05/2015**

Subject Name: Digital VLSI Design

Time: 02:30 pm to 5:00 pm **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What do you mean by MOSFET Scaling? Compare Constant Field & Constant Voltage scaling in detail.	**07**
	(b)	Draw & Explain VTC of CMOS Inverter and discuss noise margin & noise immunity in detail.	**07**
Q.2	**(a)**	Write short note on Layout Design Rules.	**07**
	(b)	Draw diagram of depletion load inverter and derive equation for noise margin.	**07**
		OR	
	(b)	For CMOS Inverter derive expression of High-to-Low Propagation delay.	**07**
Q.3	**(a)**	Explain CMOS Transmission gates with its usefulness in detail.	**07**
	(b)	Explain the need for LOCOS Process, principle of LOCOS and LOCOS process with necessary diagram.	**07**
		OR	
Q.3	**(a)**	Discuss basic principles of pass transistor circuits.	**07**
	(b)	Explain three stage CMOS Ring Oscillator Circuit in detail.	**07**
Q.4	**(a)**	Write short note on oxide related MOSFET Capacitances.	**07**
	(b)	Draw the circuit diagram & stick diagram of 2 input CMOS NOR Gate.	**07**
		OR	
Q.4	**(a)**	Explain NAND Gate using CMOS, Pass and CPL Logic.	**07**
	(b)	Draw the circuit diagram & stick diagram of 3 input CMOS NAND Gate.	**07**
Q.5	**(a)**	Draw and explain CMOS SR Latch Circuit.	**07**
	(b)	Discuss short channel effect in MOSFET with diagram.	**07**
		OR	
Q.5	**(a)**	Explain Gradual Channel Approximation and derive the equation for drain current in linear region mode and saturation mode.	**07**
	(b)	Write short note on domino logic circuit.	**07**

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