Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– I (New course)• REMEDIAL EXAMINATION – SUMMER 2015

Subject Code: 2710507 **Date:19/05/2015**

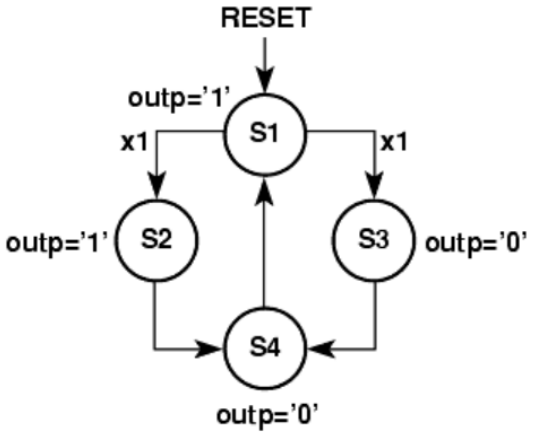
Subject Name: ASIC Design

Time: 10:30 am to 1:00 pm **Total Marks: 70**

Instructions:

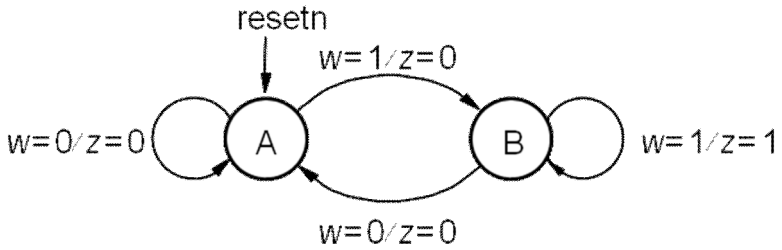
1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Do as directed. (Two marks each)	**08**
	1	Let data <= 10101100, show how it can be rotated one position right using concatenation in VHDL. Also show one position left rotation. Store result in signal a and b respectively.	
	2	Explain variable in VHDL.	
	3	What do you mean by alias?	
	4	Explain transport delay.	
	(b)	Describe significance of HDL in digital system design. State features of VHDL.	**06**
Q.2	**(a)**	Discuss FPGA architecture and explain CLBôs available in Xilinx FPGA with appropriate diagram.	**07**
	(b)	Draw programmable logic array and explain implementation of 1 bit full adder using same.	**07**
		OR	
	(b)	Discuss fuse and Anti fuse technology of FPGA programming with appropriate diagram.	**07**
Q.3	**(a)**	Discuss various data types available in VHDL with appropriate example.	**07**
	(b)	Explain configuration and package using necessary examples.	**07**
		OR	
Q.3	**(a)**	What is port mapping and how is it done? Explain with appropriate example.	**07**
	(b)	Write short note on test bench in VHDL.	**07**
Q.4	**(a)**	Explain following with appropriate example. (i) wait statement (ii) next statement	**07**
	(b)	For MOORE FSM shown in figure below, write VHDL code.	**07**



OR

Q.4	**(a)**	Explain óGenerateô statement in VHDL with an appropriate example.	**07**
	(b)	For MEALY FSM shown in figure below, write VHDL code.	**07**



Q.5 **(a)** Write VHDL code for an 8-bit Switch tail counter. It is an 8-bit shift register, where the bit 0 is inverted and fed to the D input of the bit 7. When initialized with 00000000, the sequence is 10000000, 11000000, 11100000é 00000011, 00000001. **07**

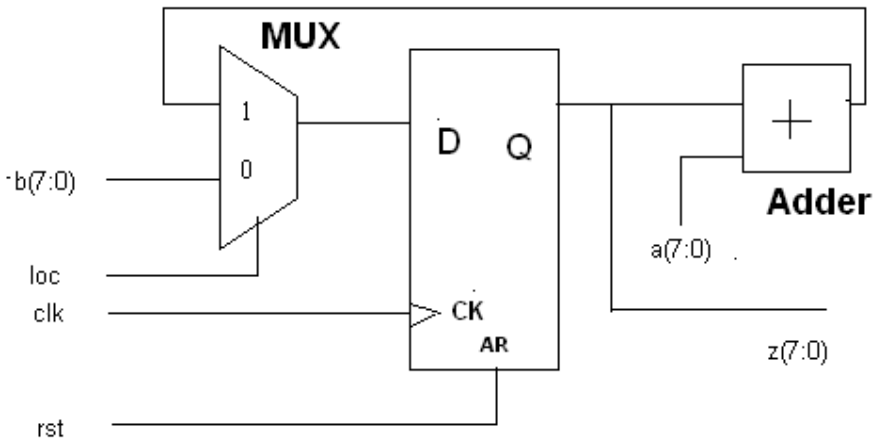
(b) For VHDL code shown below, draw circuit in terms of known combinational/sequential blocks. **07**

```
library ieee;
use ieee.std_logic_1164.all;

entity q5b is port
        (en,dir: in std_logic;
        a,b: inout std_logic_vector (3 downto 0);
end q5b;

architecture con of q5b is
begin
signal temp: std_logic_vector(1 downto 0);
        temp<=(en,dir);
                with temp select
                b<=a when ("11")
                  <=("zzzz") when others;
                with temp select
                a<=b when ("10")
                  <=("zzzz") when others;
end con;
```

OR

Q.5 **(a)** Write down the VHDL code for 4x1 multiplexer using when else construct. Using same draw diagram and write VHDL code to implement 16x1 multiplexer using structural modeling. **07**

(b) Write behavioral VHDL code for the circuit shown in figure below. (Structural style of VHDL coding is strictly not allowed.) **07**



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