Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER– I (New course)• REMEDIAL EXAMINATION – SUMMER 2015

Subject Code: 2715410 Date:16/05/2015

Subject Name: Advanced Digital Circuit Design

Time: 10:30 am to 1:00 pm Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	What is Verilog HDL? With merits and demits over other HDL List and explain major capabilities of Verilog along with the features.	**07**
	(b)	Point out difference between Moore and Mealy machine with giving a proper example	**07**
Q.2	**(a)**	Write points of difference between Blocking & Non-blocking Assignments.	**07**
	(b)	Write the Verilog code for Sequence detector for detecting ñ0110ò.	**07**
		OR	
	(b)	Write a verilog code for 4-bit ripple counter	**07**
Q.3	**(a)**	Draw the Gate level schematic and CMOS Implementation of master slave JK flip flop also draw the truth table for its operation modes of transistors.	**07**
	(b)	Give the points of difference between tasks and function Explain with suitable example.	**07**
		OR	
Q.3	**(a)**	Discuss data types used in Verilog in brief.	**07**
	(b)	Write the Verilog code to implement Digital clock	**07**
Q.4	**(a)**	Write a Verilog code for BCD to seven segment convertor	**07**
	(b)	Give the difference between combinational logic and sequential logic also write the Verilog code for ring counter	**07**
		OR	
Q.4	**(a)**	Explain Programmable Logic devices. Also Give Comparison between CPLD and FPGA.	**07**
	(b)	What is scheduling? Also briefly discuss about various scheduling algorithms.	**07**
Q.5	**(a)**	List the techniques for reducing the complexity of the digital circuit also give brief explanation with suitable flow diagram	**07**
	(b)	Explain behavioral Modeling of Verilog. Also Write Verilog code for full Subtractor using structural modeling	**07**
		OR	
Q.5	**(a)**	Discuss techniques for partitioning	**07**
	(b)	Discuss difference between modules and module instances.	**07**

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