Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–II EXAMINATION – SUMMER 2015

Subject Code: 2720314 **Date: 01/06/2015**

Subject Name: Advance VLSI Design

Time: 02:30 PM to 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Figures to the right indicate full marks.**
3. **Make suitable assumptions wherever necessary and mention it clearly in your solution.**

Q.1	**(a)**	Write verilog code to design a 4-bit adder using full adder and half adder. Use gate level modeling for half and full adders. Show synthesized output of your design.	**10**
	(b)	What do you mean by metastability? With the help of timing diagram explain how setup and hold time of flip-flop cause metastability?	**04**
Q.2	**(a)**	Write verilog code using dataflow modeling to design BCD to seven segment display assuming common anode display.	**07**
	(b)	Write verilog code using behavior modeling to design a 8-to-3 priority encoder having priority order 2, 0, 6, 7, 5, 1, 4, 3 with 2 being the highest priority input. Using a test bench check the functionality of your design.	**07**
		OR	
	(b)	Write verilog code of 2 to 4 decoder having enable input using case statement. Using a test bench check the functionality of your design.	**07**
Q.3		Consider Mealy Finite State Machine (FSM), with one input X and one output Z. The FSM asserts its output Z when it recognizes the ñ1010ò input bit sequence. Implement the state diagram for above and write verilog code for it. Using a test bench verify your design.	**14**
		OR	
Q.3		Design a counter with a binary sequence 0, 3, 2, 5, 7, 6, 0, 3, 2, é using JK flipflop. Asynchronous reset when activated, resumes counter with 0. Show all design steps. Write verilog program of the same using structural modeling style. Write verilog programs of all components used in the design. Using a test bench verify the counter design.	**14**
Q.4	**(a)**	Write verilog UDP description of negative edge triggered T-Flip-flop with active high asynchronous reset.	**07**
	(b)	Write verilog code of 2 to 4 demux using if-else-if construct. Verify your design using a test bench.	**07**
		OR	
Q.4	**(a)**	Write a verilog code for 8 bit universal shift register with shift right, shift left & parallel load capabilities.	**07**
	(b)	Write verilog code to design D latch. Using a test bench verify your design.	**07**
Q.5	**(a)**	Draw the timing diagram observed while simulating the design of x^4 implementation of pipelined architecture in Xilinx ISE that shows all signals observed in simulation window and justifies functionality of the design. State throughput, latency and timing of your design with proper justification.	**07**

(b) Implement the Boolean function Y= [{a1 (a3ô+a2)} + a5ô] a4 using minimum area as an optimization constraint. Consider that synchronous set and reset D-flipflops are available as the FDS element in the device. Write Verilog code and draw implementation diagram of the same. What are the throughput, latency and timing of your design? How? **07**

OR

Q.5 **(a)** An FIR filter operation Z<= Px + Qx1 + Rx2 + Sx3, where P, Q, R, S are filter coefficients and x1 = x(n-1), x2 = x(n-2), x3 = x(n-3) are input samples, needs tobe implemented using pipelined architecture having timing constraint of one 8 bit x 8 bit multiplier only. Write verilog code and draw implementation diagram. What is throughput and latency of your design ? **07**

(b) Write verilog code and implementation diagram to implement following functionality by using logical reordering to reduce critical path in the design. Assume critical path is between r and Y. **07**

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if (Condition1)   Y<= p
else if (Condition2 && (r>7) )   Y<= q
else  Y<= r
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