Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

ME - SEMESTER–II EXAMINATION – SUMMER 2015

Subject Code: 2720511 **Date: 05/06/2015**

Subject Name: CMOS CIRCUIT DESIGN - I

Time: 02:30 PM to 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Figures to the right indicate full marks.**
3. **Make suitable assumptions wherever necessary and mention it clearly in your solution.**

Q.1	**(a)**	Describe the MOS small signal model.	**07**
	(b)	Explain I/V characteristic of MOS.	**07**
Q.2	**(a)**	Explain input output characteristic of CS configuration.	**07**
	(b)	Explain difference between single ended and differential operation.	**07**
		OR	
	(b)	Explain cascode current mirrors.	**07**
Q.3	**(a)**	What aspects of the performance of an amplifier are important?	**07**
	(b)	Explain common source stage with diode connected load.	**07**
		OR	
Q.3	**(a)**	Explain Gilbert cell.	**07**
	(b)	Describe and analyze the CMOS inverter.	**07**
Q.4	**(a)**	Explain in short (i) Threshold voltage (ii) Noise margin. (iii) Circuit design levels.	**07**
	(b)	Explain basic differential pair and analysis.	**07**
		OR	
Q.4	**(a)**	Describe the two stage op-amp and define slew rate & common mode feedback.	**07**
	(b)	Explain cascode current mirrors circuit.	**07**
Q.5	**(a)**	Explain 3 ï stage ring oscillator.	**07**
	(b)	Explain differential pair with MOS load.	**07**
		OR	
Q.5	**(a)**	Describe the frequency response of source followers.	**07**
	(b)	Explain compensation of two stage op amp and also explain other compensation techniques.	**07**

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